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(71) Applicant: MOTOROLA, INC. [US/US], 1303 East Algonquin Road, Schaumburg, IL 60196 (US)

(72) Inventors: MADHUKAR, Sucharita, 1902 Cervin Boulevard, Austin, TX 78728 (US) NGUYEN, Bich-Yen, 110 Laurelwood Drive, Austin, TX 78733 (US)

(74) Agents: GODDARD, Patricia, S., Motorola Corporate Law Department, 7700 West Parmer Lane, TX32/PL02__, Austin, TX 78729 et al (US)

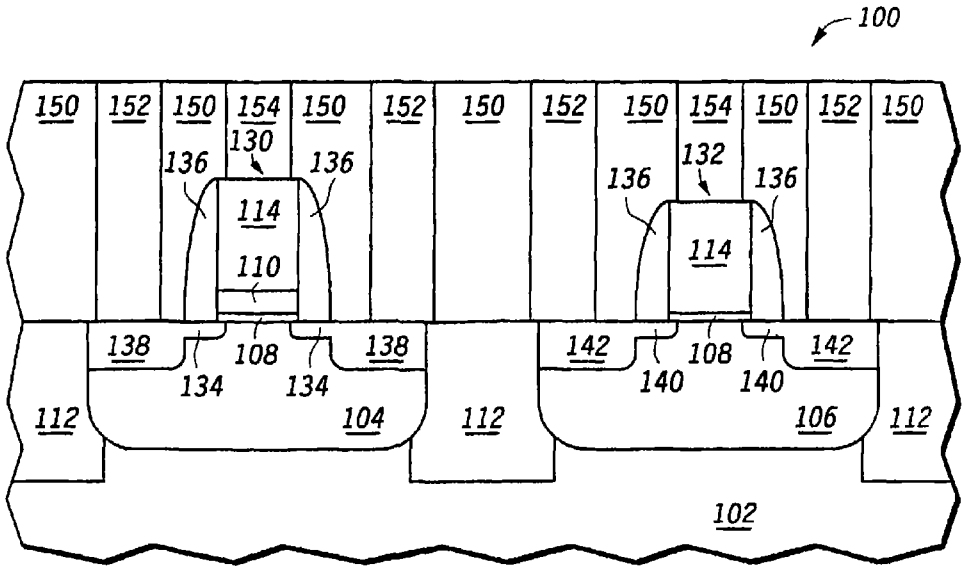
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Title: DUAL METAL GATE TRANSISTORS FOR CMOS PROCESS



(57) **Abstract:** A process for forming a first transistor (130) of a first conductivity type and a second transistor (132) of a second conductivity type in a semiconductor substrate (102) is disclosed. The substrate (102) has a first well (106) of the first conductivity type and a second well (104) of the second conductivity type. A gate dielectric (108) is formed over the wells. A first metal layer (110) is then formed over the gate dielectric (108). A portion of the first metal layer (110) located over the second well is then removed. A second metal layer (114) different from said first metal is then formed over the wells and a gate mask is formed over the second metal (114). The metal layers (110, 114) are then patterned to leave a first gate over the first well (106) and a second gate over the second well (104). Source/drains (138, 142) are then formed in the first (106) and second (104) wells to form the first (130) and second (132) transistor.

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