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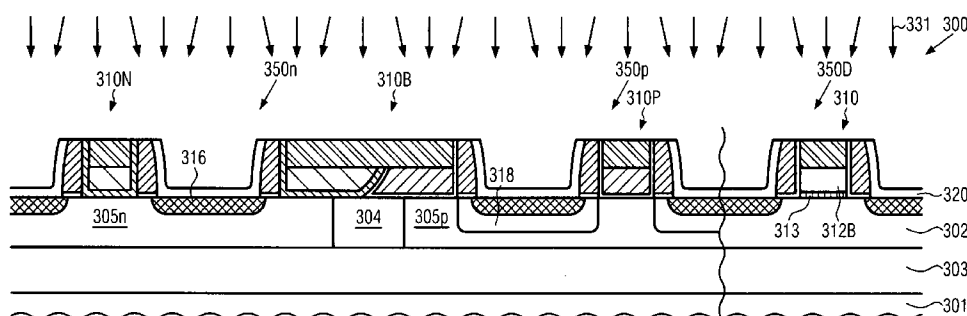


FIG. 3p

(57) Abstract: In the process sequence for replacing conventional gate electrode structures (310) by high-k metal gate structures (310N, 310B, 310P), the number of additional masking steps may be maintained at a low level, for instance by using highly selective etch steps (322, 325, 327, 331), thereby maintaining a high degree of compatibility with conventional CMOS techniques. Furthermore, the techniques disclosed herein enable compatibility to front-end process techniques and back-end process techniques, thereby allowing the integration of well-established strain-inducing mechanisms in the transistor level as well as in the contact level.