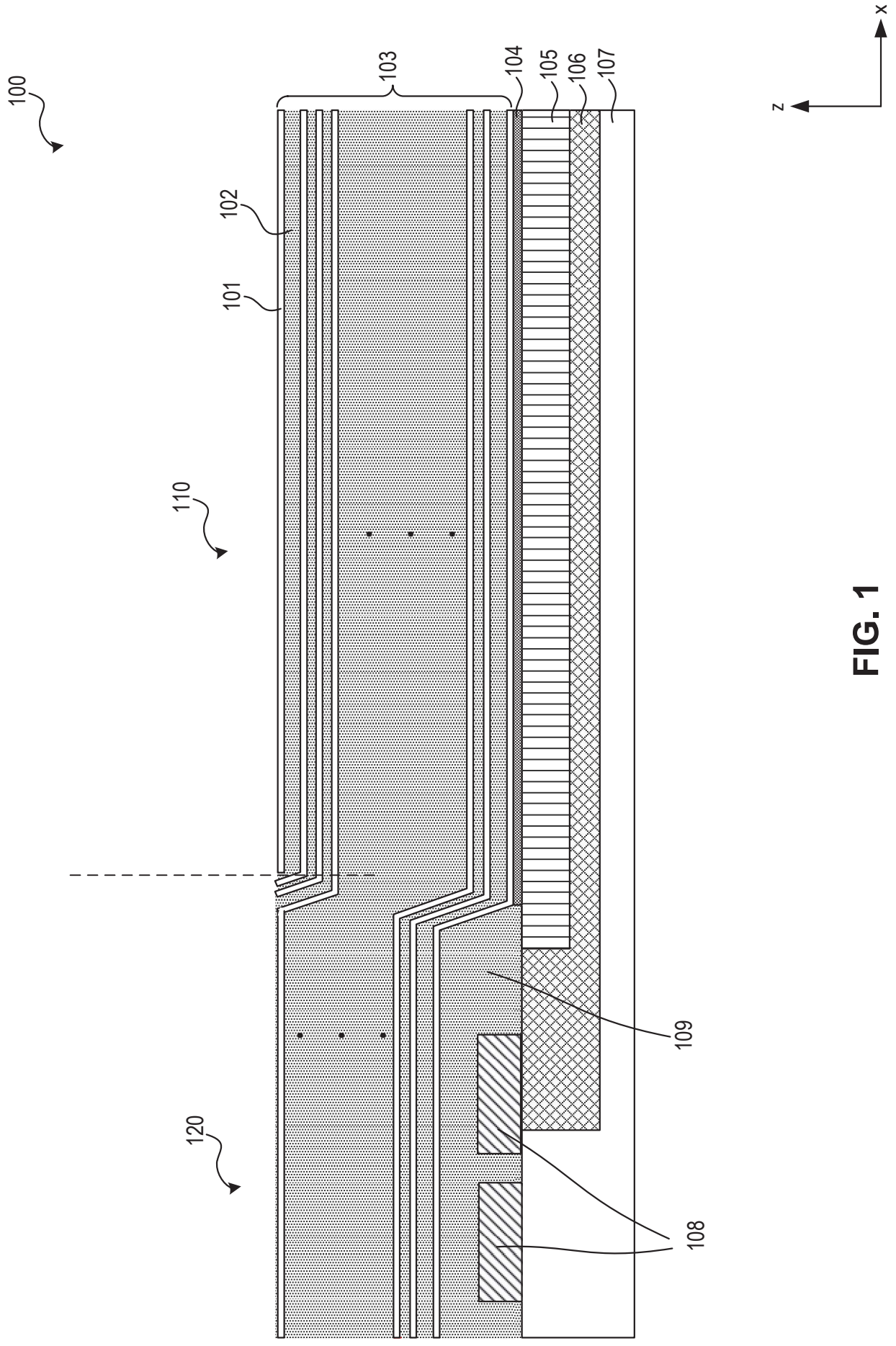

FIG. 1

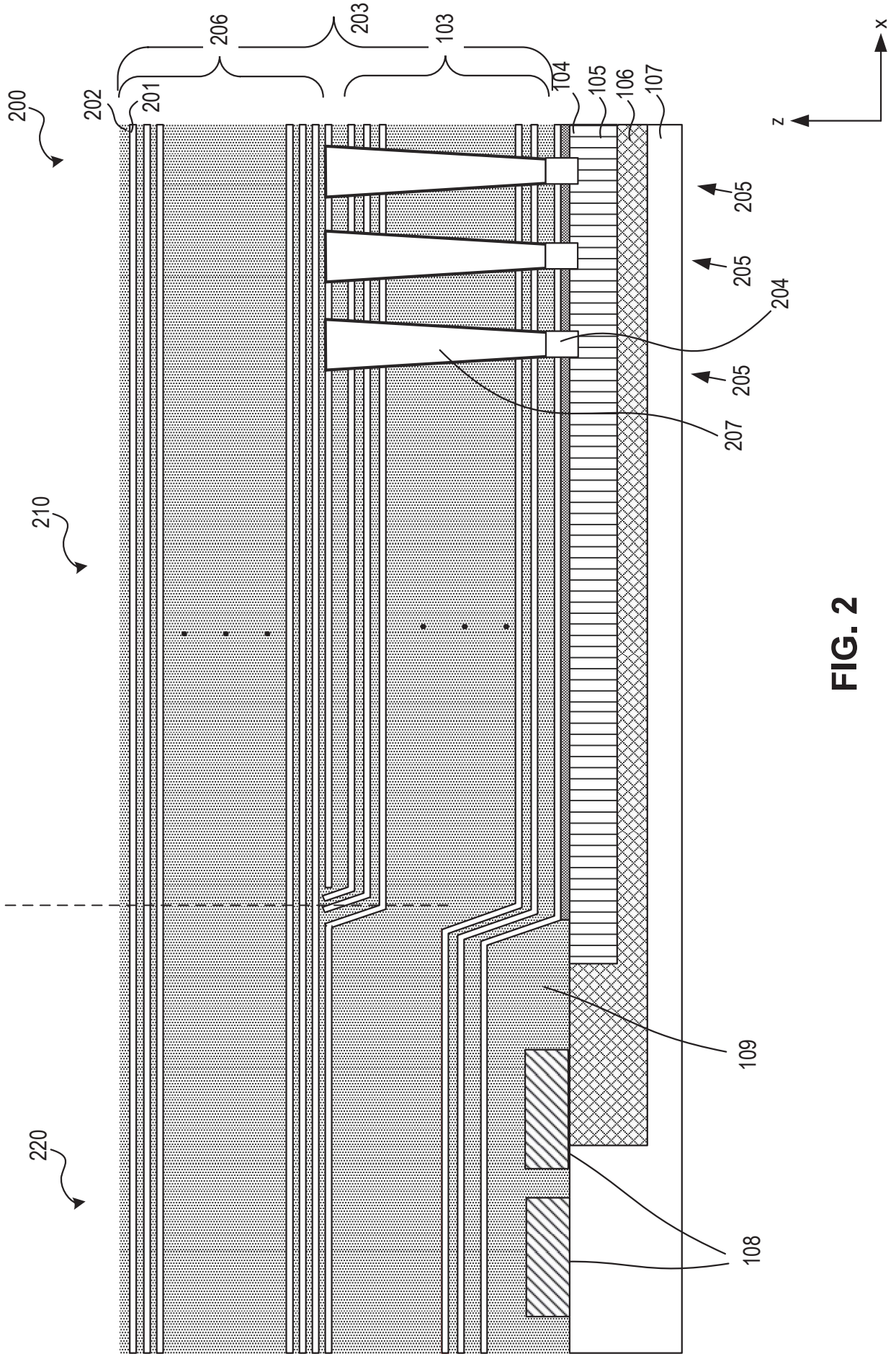
200
202
201
206
203
103
104
105
106
107
x
z
205
205
205
204
207
210
220
109
108

FIG. 2

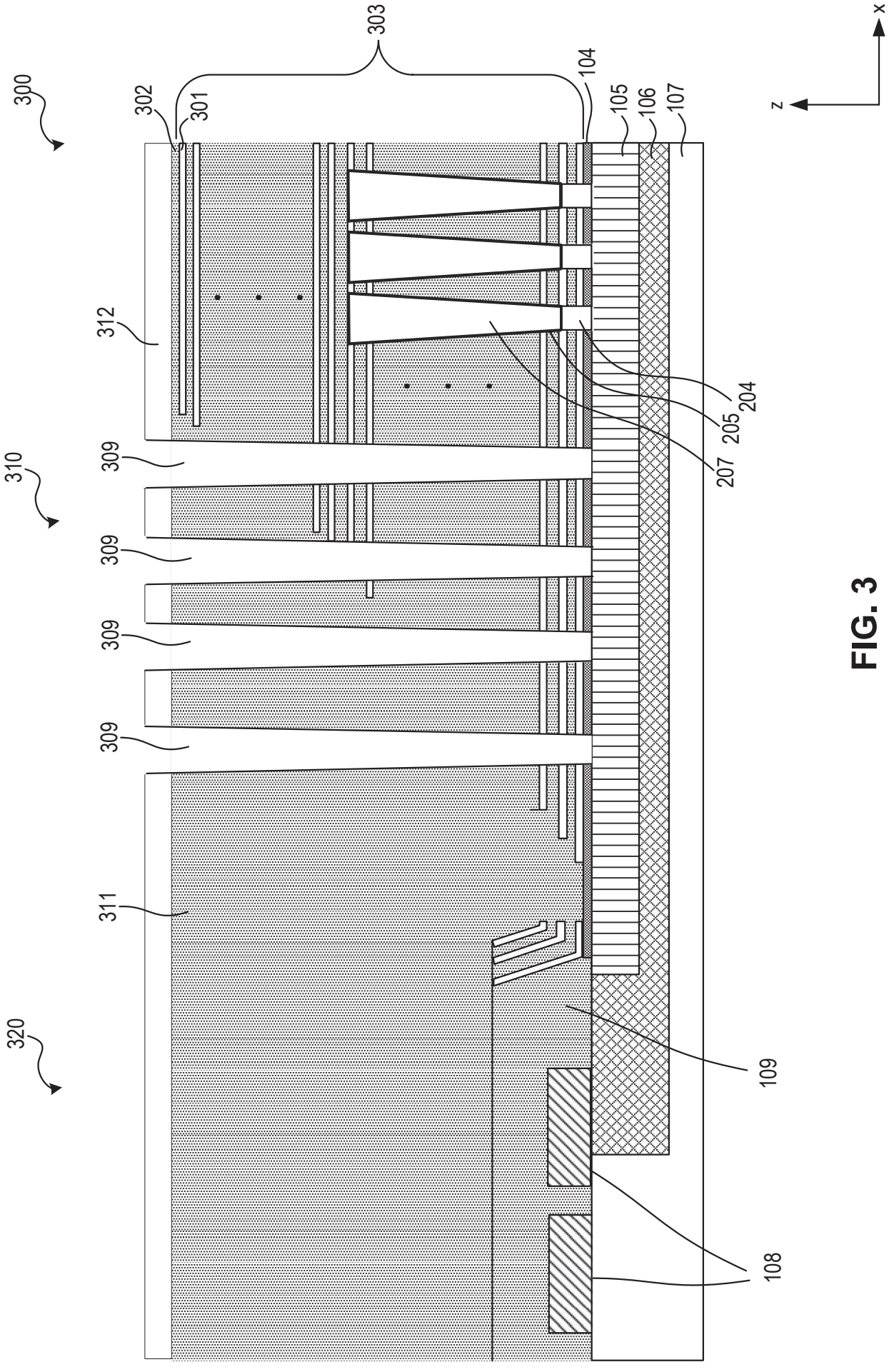
300
302
301
303
104
105
106
107
x
z
312
204
205
207
310
309
309
309
309
311
320
109
108

FIG. 3

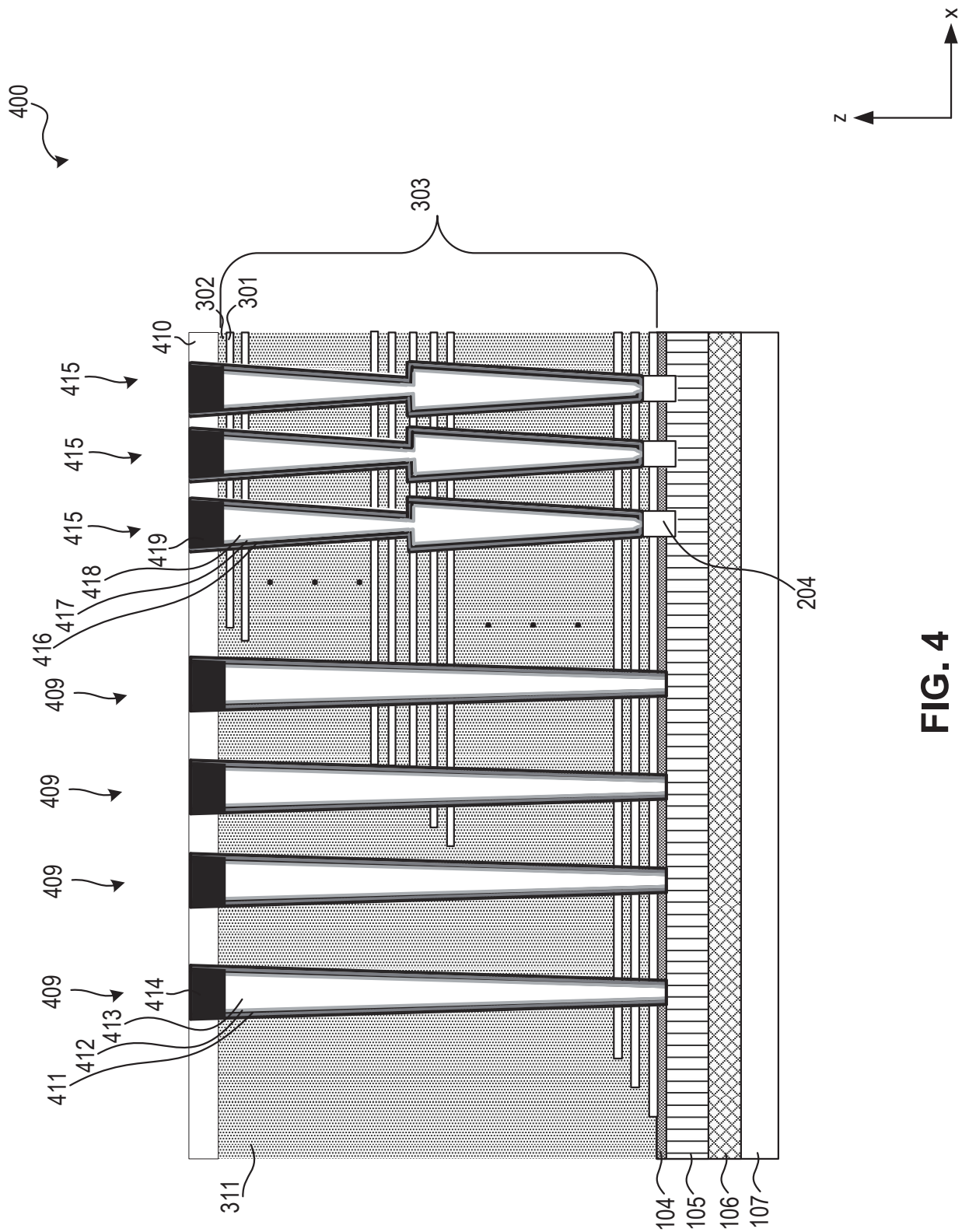
400
303
302
301
410
415
415
415
419
418
417
416
409
409
409
409
414
413
412
411
204
311
104
105
106
107
x
z

FIG. 4

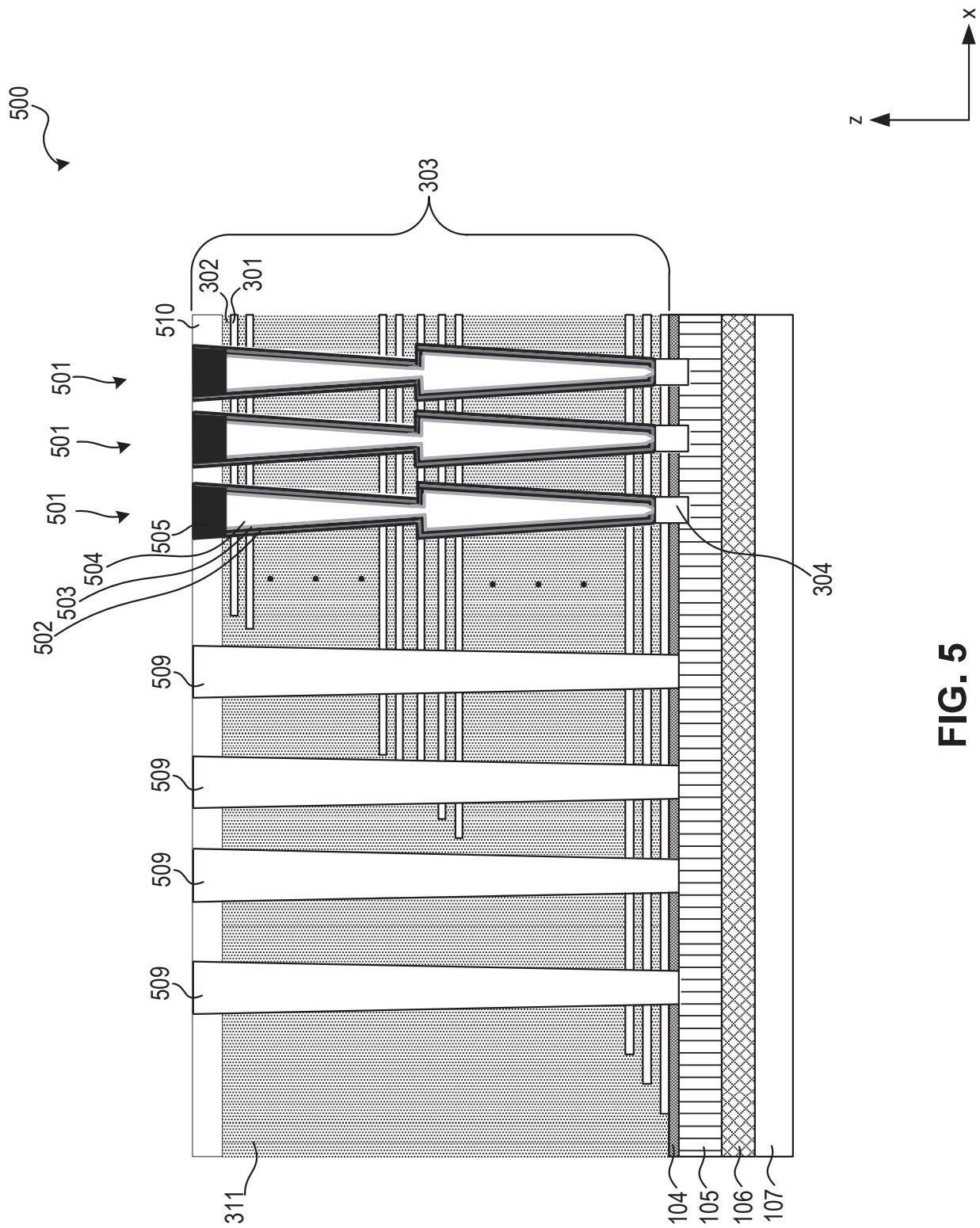
500
303
302
301
510
501
501
501
505
504
503
502
509
509
509
509
304
311
104
105
106
107
x
z

FIG. 5

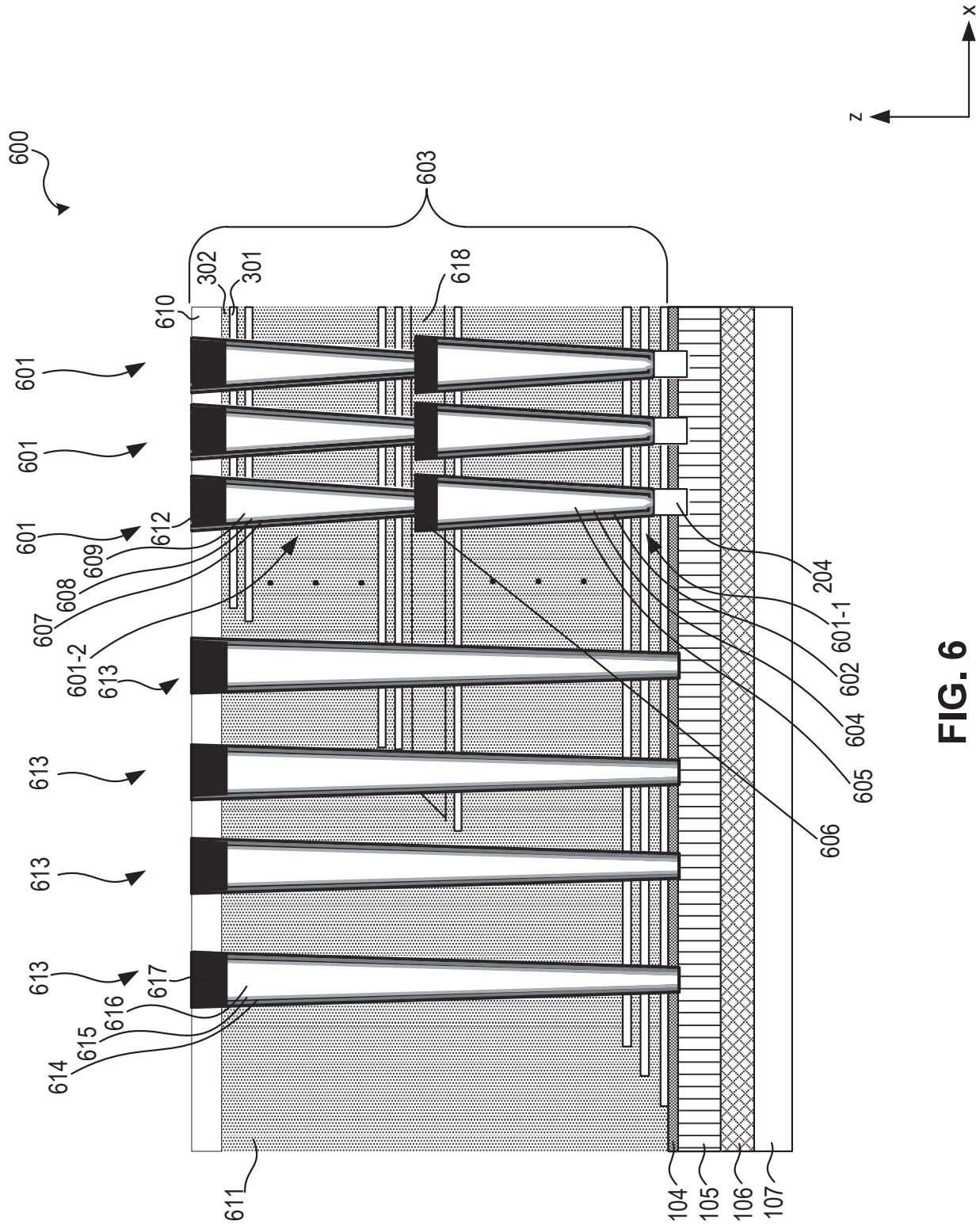
600
603
302
301
618
610
601
601
601
612
609
608
607
601-2
613
613
613
613
617
616
615
614
611
204
601-1
602
604
605
606
104
105
106
107
x
z

FIG. 6

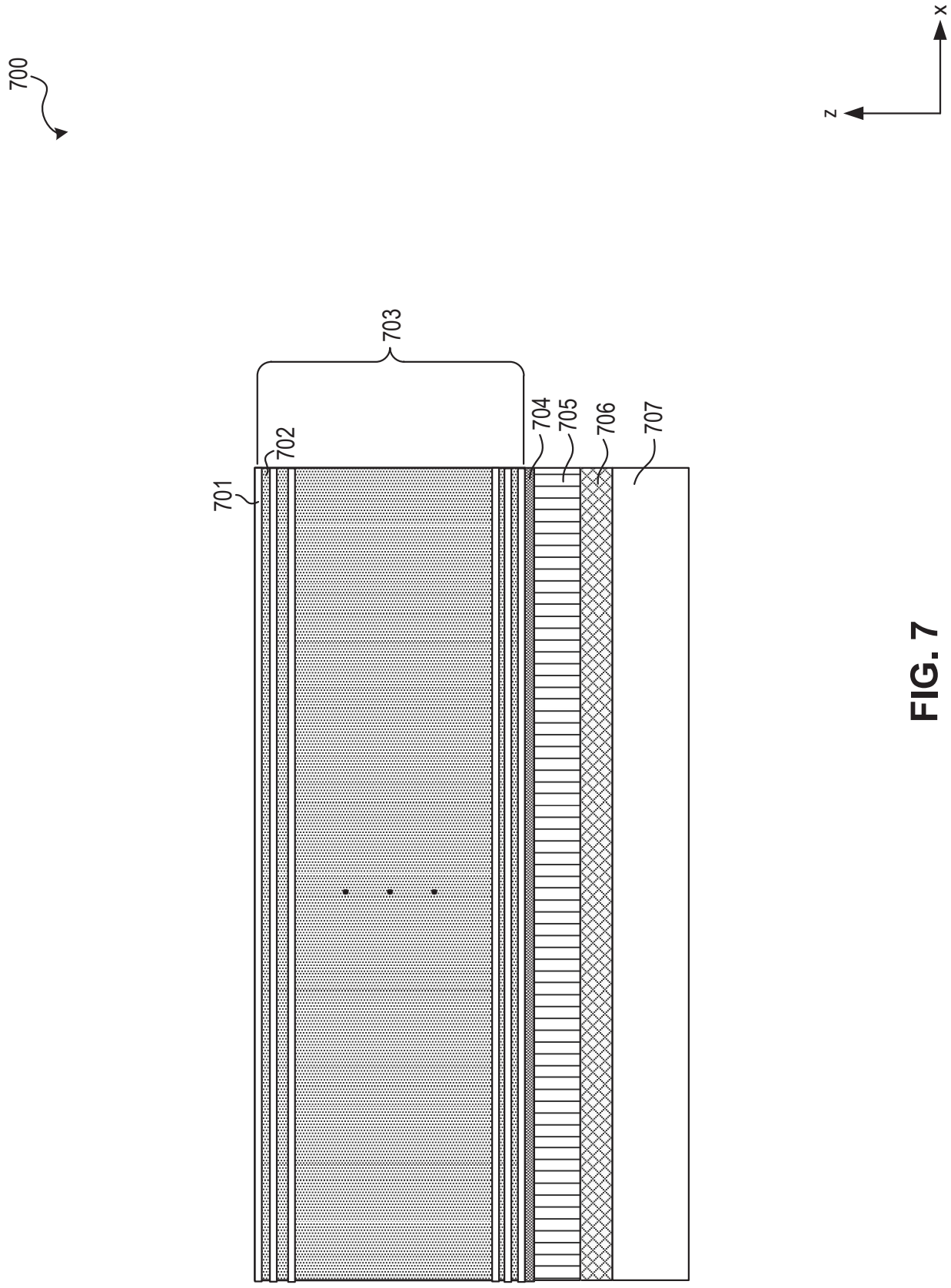

FIG. 7

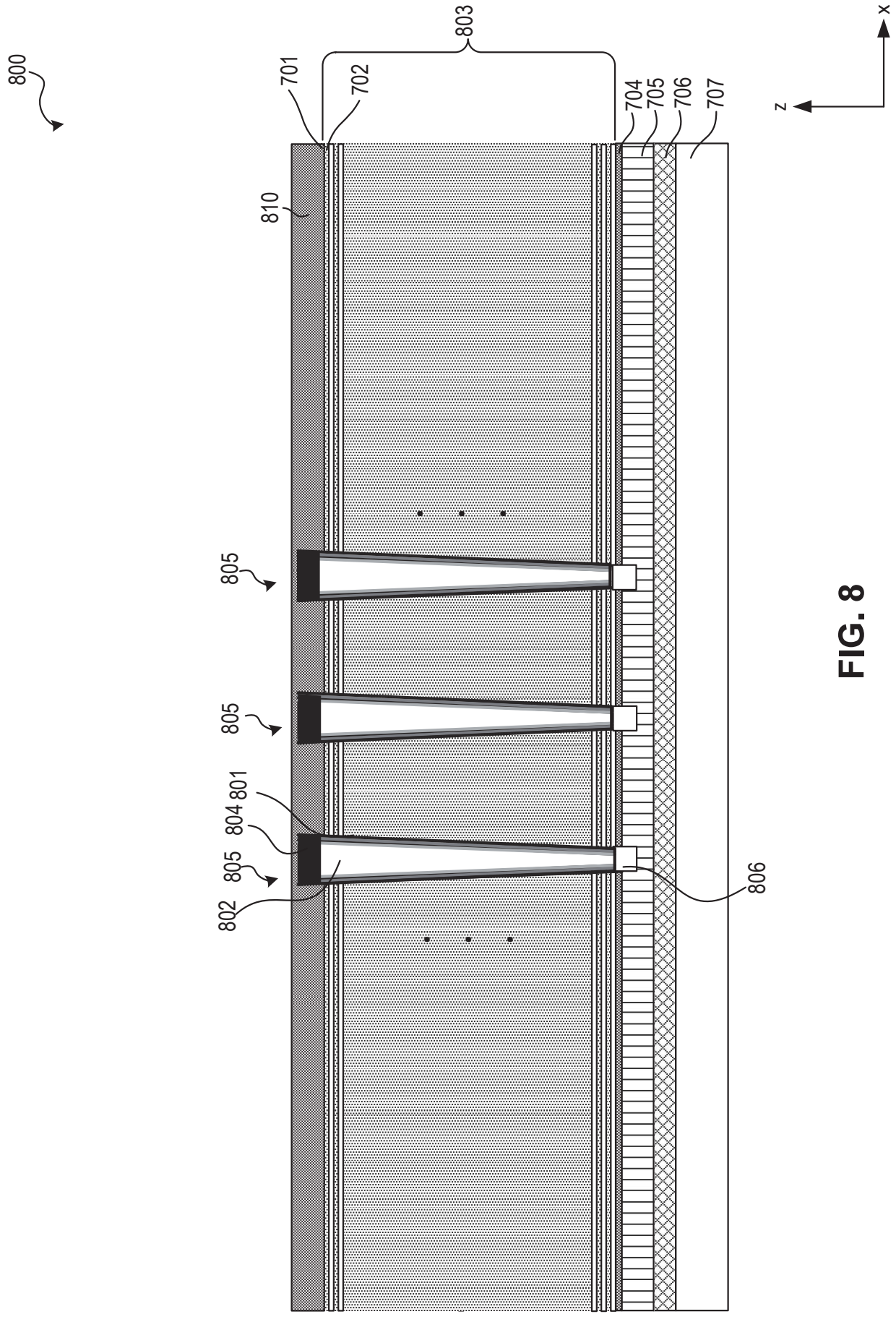
800
803
701
702
704
705
706
707
x
z
810
805
805
801
804
805
802
806

FIG. 8

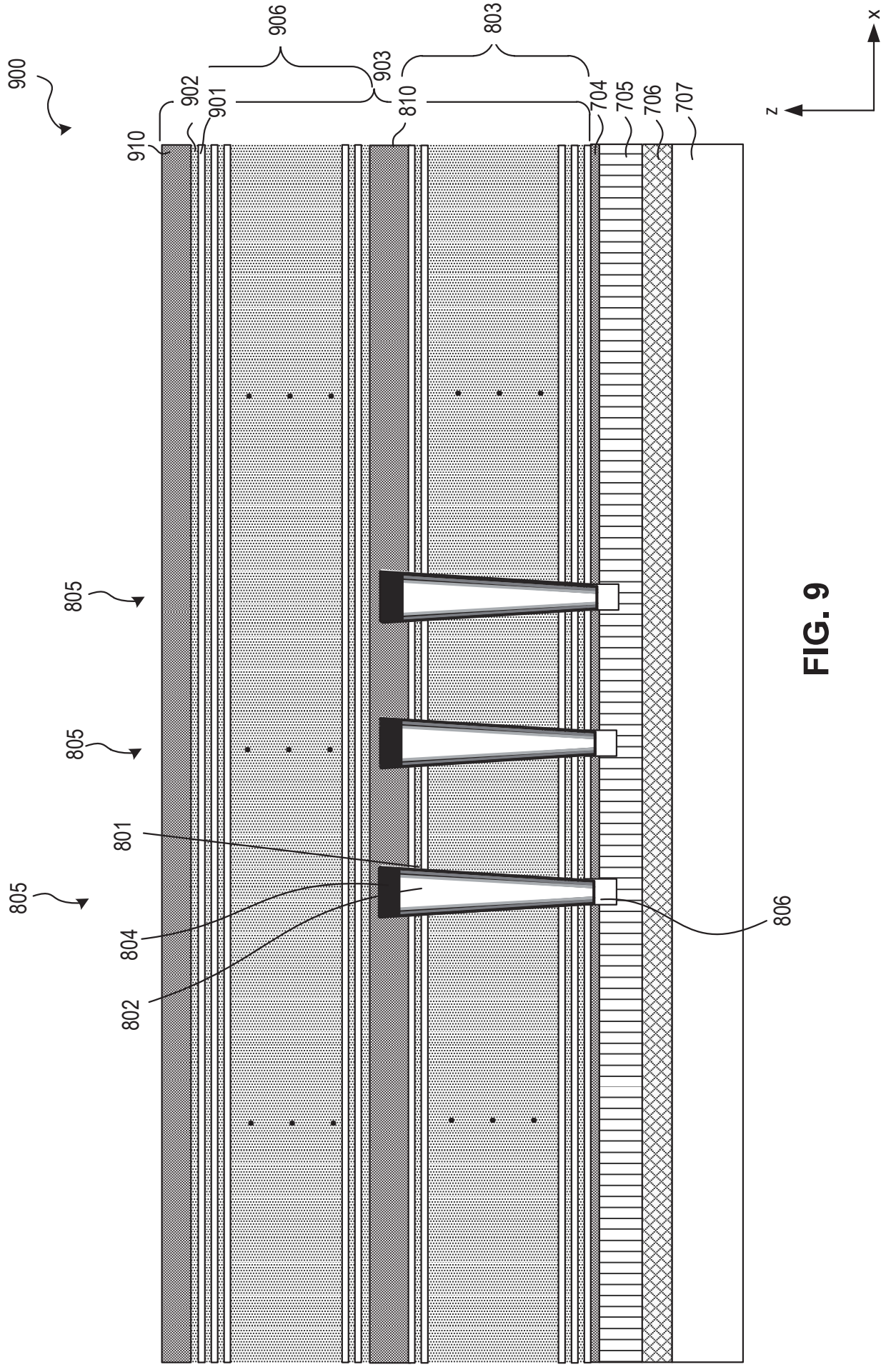
900
906
903
902
901
910
803
810
704
705
706
707
x
z
805
805
805
801
804
802
806

FIG. 9

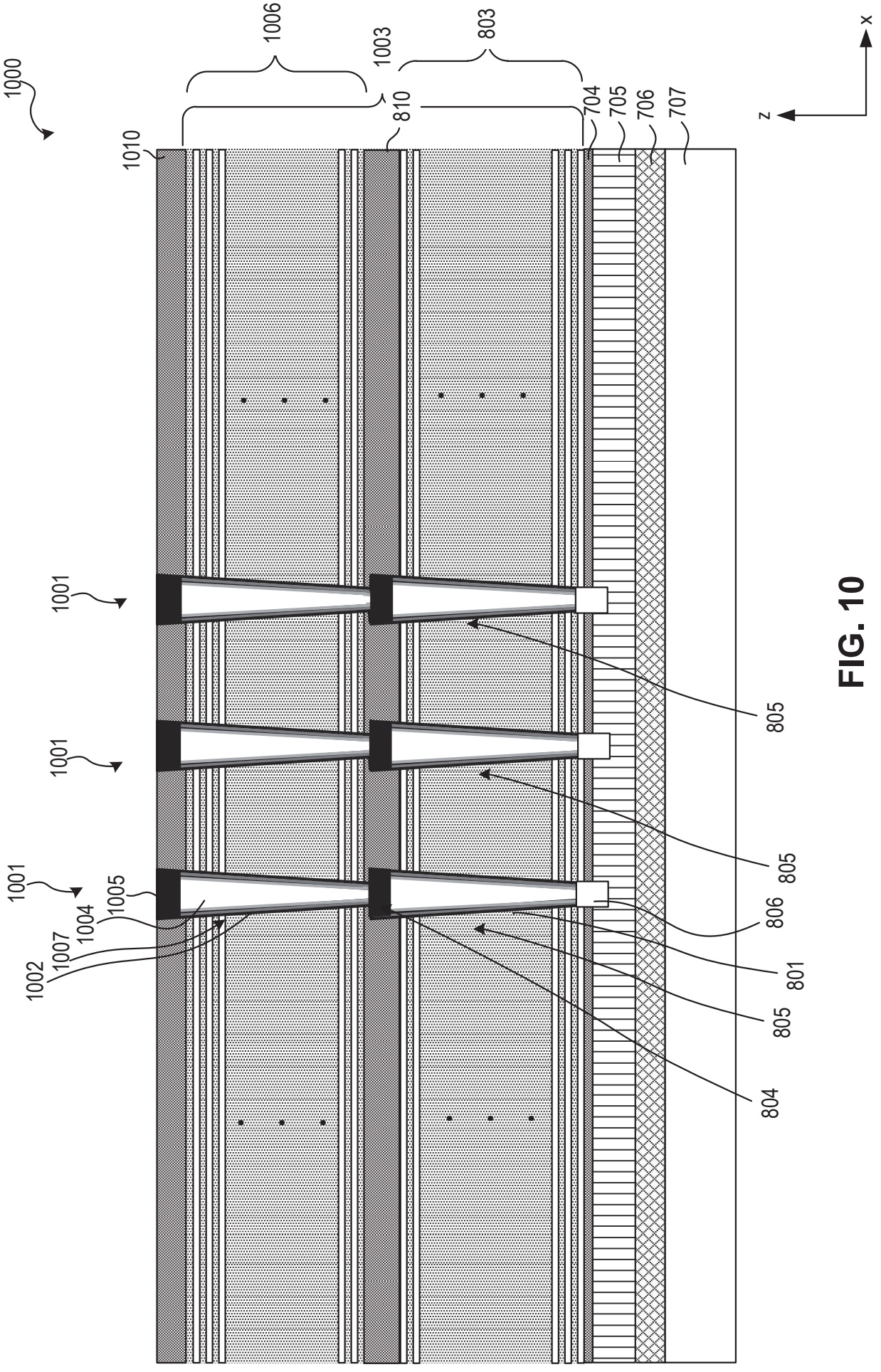
1000
1006
1003
803
810
704
705
706
707
1010
x
z
1001
1001
1001
805
805
806
801
805
804
1005
1004
1007
1002

FIG. 10

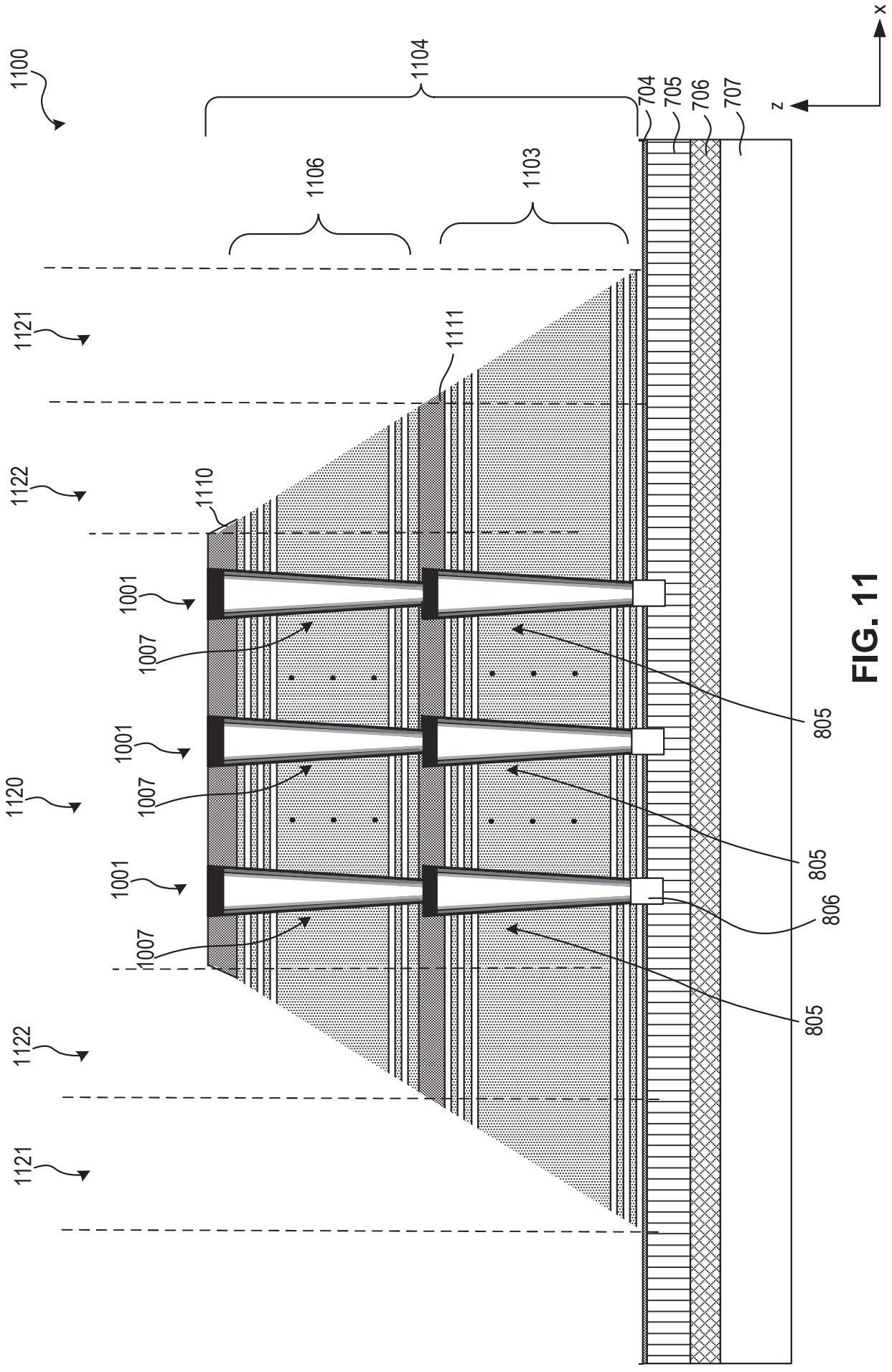
1100
1104
704
705
706
707
x
z
1106
1103
1121
1111
1122
1110
1001
1007
805
1120
806
1122
1121

FIG. 11

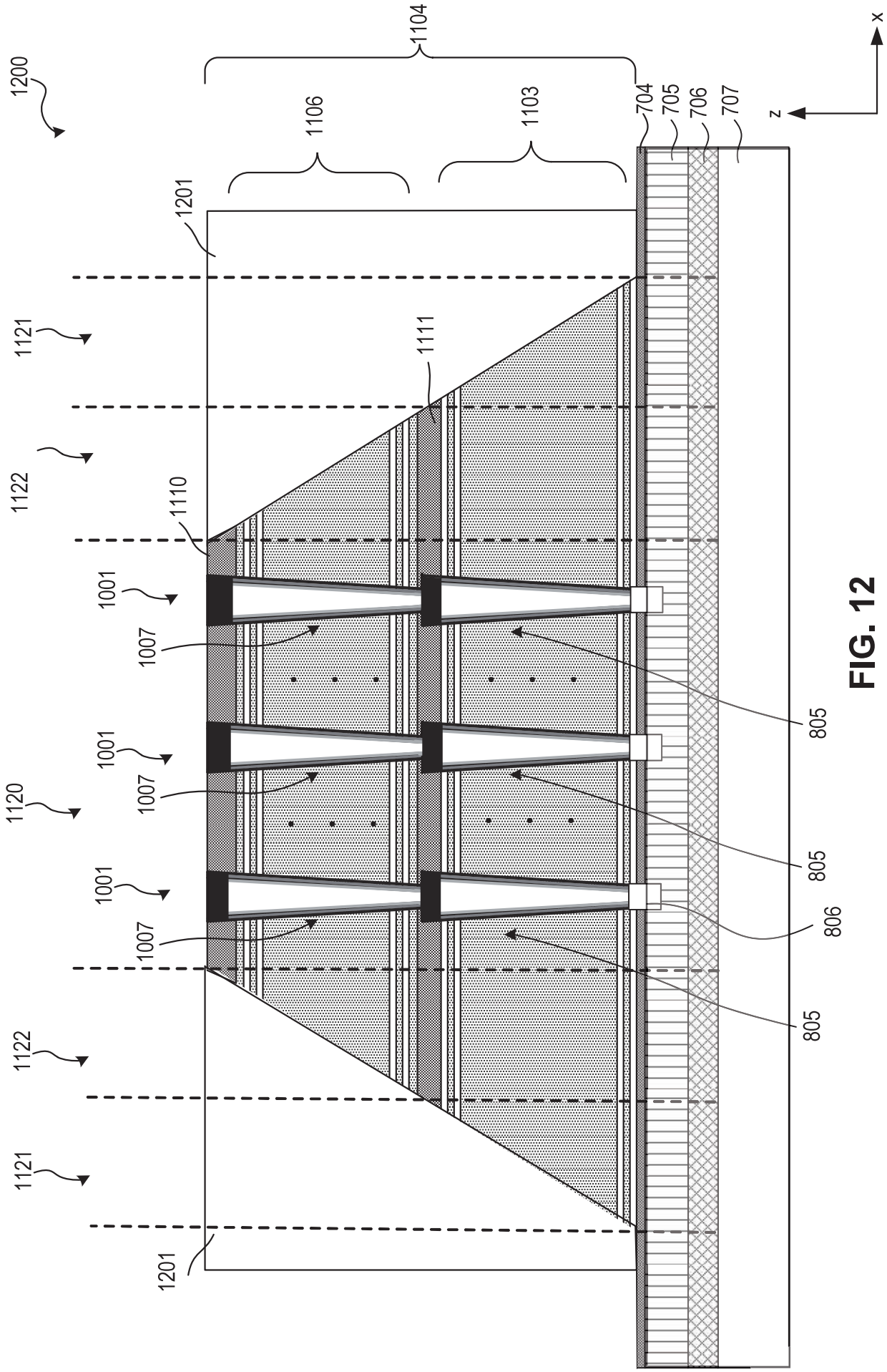
1200
1104
1106
1103
704
705
706
707
x
z
1201
1121
1111
1122
1110
1001
1007
805
1120
806
1201

FIG. 12

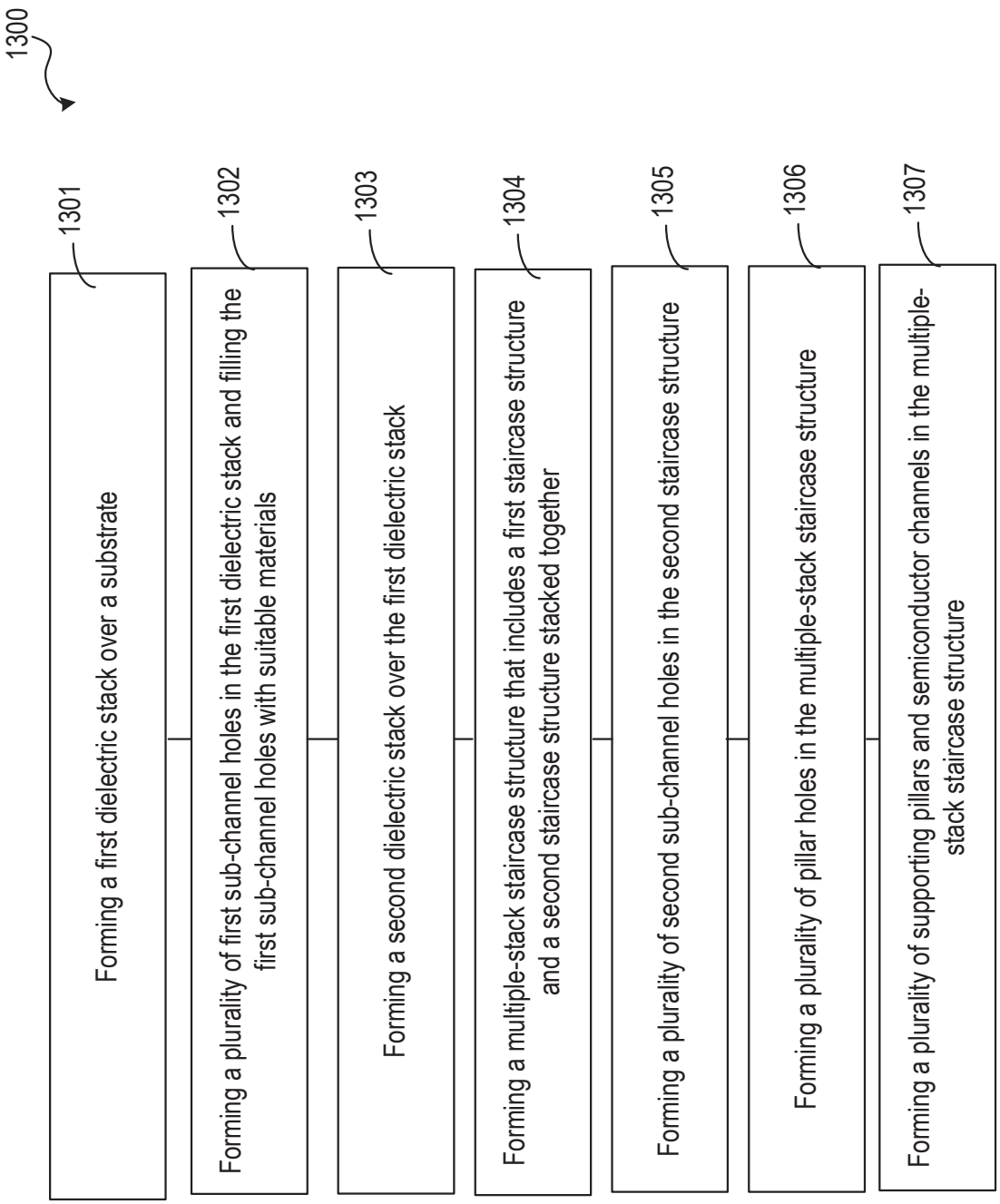
1300
1301
Forming a first dielectric stack over a substrate
1302
Forming a plurality of first sub-channel holes in the first dielectric stack and filling the first sub-channel holes with suitable materials
1303
Forming a second dielectric stack over the first dielectric stack
1304
Forming a multiple-stack staircase structure that includes a first staircase structure and a second staircase structure stacked together
1305
Forming a plurality of second sub-channel holes in the second staircase structure
1306
Forming a plurality of pillar holes in the multiple-stack staircase structure
1307
Forming a plurality of supporting pillars and semiconductor channels in the multiple-stack staircase structure

FIG. 13