MOSFETS COMPRISING SOURCE/DRAIN REGIONS WITH SLANTED UPPER SURFACES, AND METHOD FOR FABRICATING THE SAME

ABSTRACT

The present invention relates to improved metal-oxide-semiconductor field effect transistor (MOSFET) devices comprising source and drain (S/D) regions having slanted upper surfaces (14A, 16A) with respect to a substrate surface. Such S/D regions may comprise semiconductor structures that are epitaxially grown in surface recesses in a semiconductor substrate (10). Each surface recess preferably has a bottom surface (14, 16) that is parallel to the substrate surface (10A), which is oriented along one of a first set of equivalent crystal planes, and one or more sidewall surfaces (14A, 16A) that are oriented along a second, different set of equivalent crystal planes. The slanted upper surfaces (14A, 16A) of the S/D regions function to improve the stress profile in the channel region as well as to reduce contact resistance of the MOSFET. Such S/D regions with slanted upper surfaces (14A, 16A) can be readily formed by crystallographic etching of the semiconductor substrate (10), followed by epitaxial growth of a semiconductor material.

Fig. 2.



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