

ABSTRACT

Memory controllers, memory devices, and memory systems are disclosed. In an embodiments, a memory system includes a memory device configured to provide a data processing function such as a computational function. In the memory system, during at least a part of a period in which some ranks among N ranks sharing a data channel perform a computational operation, at least one of the remaining ranks performs a general memory operation such as a write or read operation, allowing the memory system to reduce delays in the general memory operation while still providing the computational operation.

FIG. 1