

Description

Background of the Invention

Field of the Invention

This invention relates generally to bipolar memory cells and, more particularly, to bipolar memory cells having an AC transient driver for improving the downward transition of the row select line without substantially increasing power requirements.

Background Art

Memory cells are circuits wherein information may be stored in a low current stand-by mode and may be written or read in a higher current mode. A typical bipolar memory cell is illustrated in FIG. 1 and is also described in detail in the detailed description of the preferred embodiment. This previously known circuit comprises a plurality of memory cells wherein each typically includes a pair of multi-emitter transistors coupled between a row select line and a current drain line to function as a latch in a manner well known to those skilled in the art. Resistive loads are coupled between each transistor and the row select line. A row driver transistor is coupled between a first supply voltage terminal and the row select line and is responsive to a select signal. A current source transistor is coupled between the current drain line and a second supply voltage terminal.

A first and second discharge transistor are coupled between the row select line and the current drain line, respectively, and the second supply voltage terminal. A first diode is coupled between the row select line and the first discharge transistor and a second diode is coupled between the current drain line and the second discharge transistor.

Another previously known method similar to the above method includes logic circuitry for determining when the downward transition occurs, and which sends additional current to the NPN current source transistor 22 for a speedier discharge of the inherent capacitance. However, this method requires additional current and sophisticated timing which are extremely detrimental in memory cells, especially as the size of memory increase.

Yet another method of discharging the row select line and the current drain line is disclosed in UK Patent Application 2 117 202A, and includes a PNP transistor responsive to the potential developed at the row select line for biasing an NPN transistor, wherein the collector-emitter conduction path of the latter is coupled to the row select line or the current drain line for draining the current therefrom. In addition, European Patent Application 0 056 206 discloses still another method of discharging these lines.

Thus, what is needed is an improved AC transient driven circuit for memory cells that provides an improved downward transition without a requirement for additional power.

Summary of the Invention

Accordingly, it is an object of the present invention to provide an improved row line driver circuit which allows memory cells to be deselected with improved downward transition without an increased power requirement.

In accordance with the invention, there is provided a memory circuit, comprising:

a plurality of memory cells coupled between a selection line and a current drain line;

first means responsive to a select signal and coupled to said selection line for providing current to said plurality of memory cells;

a first transistor having a base, an emitter and a collector, said base being responsive to said select signal, said collector being coupled to a first source of operating potential;

current supply means for providing a current of predetermined magnitude;

a second transistor having a base, an emitter and a collector, said base and collector being coupled together to said current supply means;

second means coupled in series with the first and second transistors for conducting substantially the same current as flowing through said plurality of memory cells for the steady state of said select signal which develops a potential thereacross substantially equal to the potential developed across said plurality of memory cells; and

a third transistor having a base, an emitter and a collector, said collector being coupled to a second source of operating potential, said emitter being coupled to said current drain line for sinking current therefrom, said base being coupled to said collector of said second transistor, wherein said current sunk through said third transistor is substantially equal to said current provided by said current supply means for the steady state of said select signal, said current sunk through said third transistor being substantially equal to said current provided by said current supply means multiplied by the beta thereof for the transitions of said select signal.

According to a first embodiment, the second means may be coupled between the emitters of the first and second transistors.

According to a second embodiment, the second means may be coupled between the collector of the second transistor and the current supply means, the emitter of the second transistor being coupled to the emitter of the first transistor. Preferably, the second means further includes capacitive means coupled between the base of the second transistor and the base of the third transistor.

Brief Description of the Drawings

FIG. 1 is a schematic of a typical bipolar memory cell in a row selection configuration.

FIG. 2 is a graph illustrating selection and deselection of the memory cell of FIG. 1.

FIG. 3 is a schematic of a first embodiment of the present invention.

FIG. 4 is a schematic of a second embodiment of the present invention.

Detailed Description of the Preferred Embodiment

Referring to FIG. 1, a previously known circuit includes a pair of cross-coupled multi-emitter transistors 11, 12 which function as a latch. The bases of transistors 11, 12 are coupled to each others collector. A first emitter of each transistor 11, 12 is connected to a stand-by current drain line 13. A second emitter of transistor 11 is connected to bit line 14 and a second emitter of transistor 12 is connected to bit line 15. The collectors of transistors 11, 12 are coupled to row select line 16 by resistors 17, 18, respectively.

This memory cell is one of a plurality of memory cells that would be coupled between row select line 16 and current drain line 13. For instance, for a 16K memory, there could be 128 memory cells connected to each row select line 16.

An NPN row driver transistor 19 has an emitter connected to row select line 16, a collector connected to reference voltage line 21 and a base adapted to receive input signal V_s . An NPN current source transistor 22 has a collector connected to stand-by current drain line 13, an emitter coupled to reference voltage line 23 by resistor 24, and a base adapted to receive bias voltage V_B .

When input signal V_s is positive, or transitioning upward, the NPN row driver transistor 19 provides current to row select line 16 charging all internal node capacitances and discharge line 13 to the selected voltage potential. Due to the β multiplication of the NPN transistors, this positive transition occurs relatively rapidly.

When input signal V_s is negative, or transitioning downward, NPN row driver transistor 19 no longer supplies current to row select line 16. Current source transistor 22 will drain capacitive charge from the memory cell.

However, inherent capacitances from the collector of the cross-coupled transistors 11, 12 and row select line 16 to ground and between the base-emitter of cross-coupled transistors 11, 12 causes this cell transition to be slow when discharged with the standby current source, transistor 22.

Previously known attempts to increase the speed of this downward transition include the addition of diode 25 coupled between row select line 16 and the collector of NPN accelerate discharge transistor 26. Transistor 26 has an emitter coupled to ground by resistor 27 and a base adapted to receive bias voltage V_{BB} . Diode 28 is coupled between current drain line 13 and the collector of NPN transistor 29. Transistor 29 has an emitter coupled to ground by resistor 31 and a base adapted to receive bias voltage V_{BB} . As the voltage on row select line 16 and current drain line 13 transitions downward, transistors 26, 29 accelerate this downward transition by helping to remove the stored charge from the inherent cell capacitances.

The currents in transistors 26, 29 are many times the current in each individual memory cell. These currents are diode logic steered by circuitry not shown to the appropriate row to aid in its discharge until another row is selected and exceeds the falling deselected row's voltage. The rate of fall decreases at cell switchover as the rising cell picks up the current resulting in slow full deselect of the cell.

Referring to FIG. 2, waveform 32 illustrates an upper transition for the voltage on row select line 16 for a positive transitioning select signal V_s to the base of transistor 19. Waveform 33 illustrates a downward transition for the voltage on row select line 16 for a negative transitioning select signal V_s to the base of transistor 19. At the cross-over point 34 of waveforms 32, 33, the downward rate of waveform 33 tapers off dramatically. The dotted waveform 35 represents a more desirable path.

Referring to FIG. 3, the preferred embodiment of the present invention includes a pair of cross-coupled multi-emitter transistors 41, 42 that have collectors cross-coupled to each others base and coupled to row select line 43 by resistors 44, 45, respectively. A first emitter of each transistor 41, 42 is connected to stand-by current drain line 46. A second emitter of transistor 41 is connected to bit line 47 and a second emitter of transistor 42 is connected to bit line 48.

Resistors 44, 45 are only by way of example. Diodes may be substituted for resistors 44, 45 or a resistor and diode may be placed in parallel. Further alternatives would include transistors coupled between the collectors of transistors 41, 42 and row select line 43.

As in the previously described memory array of FIG. 1, a plurality of memory cells would actually be coupled between row select line 43 and current drain line 46. This plurality of memory cells is reflected by dotted lines for row select line 43 and current drain line 46.

NPN row driver transistor 49 has an emitter coupled to row select line 43, a collector connected to reference voltage line 51, and a base adapted to receive select signal V_s . NPN transistor 52 has its collector connected to reference voltage line 51 and its base adapted to receive select signal V_s . The emitter of transistor 52 is coupled to the collector of transistor 53 by resistor 54 and to the base of transistor 53 by resistor 55. The emitter of transistor 53 is connected to the emitter of PNP transistor 56. Both the base and collector of transistor 56 are connected to the base of PNP transistor 57 and are coupled to ground by current source 58. The collector of transistor 57 is also connected to ground. Transistor 53 and resistors 54, 55 comprise a half cell and will draw a substantially similar current to that of the memory cell comprising transistors 41, 42 and resistors 44, 45. The half cell and memory cell may be of any type. The main requirement is that their currents are substantially similar. Transistors 56 and 57 are matched and will draw a substantially similar current. Current source 58

sets the current level in all devices.

When a negative, or downward transition, select signal V_s is applied to the bases of transistors 49, 52, transistors 49, 52 will turn off. Current source 58 will pull down transistors 56, 57. Transistor 57 will pull down the row memory cells with current I multiplied by β .

Referring to FIG. 4, a second embodiment of the present invention comprises a pair of cross-coupled multi-emitter transistors 61, 62 having their collectors cross-coupled to each others base and coupled to row select line 63 by resistors 64, 65, respectively. A first emitter of each transistor 61, 62 is connected to stand-by current drain line 66. A second emitter of transistor 61 is connected to bit line 67 and a second emitter of transistor 62 is connected to bit line 68. As with the memory cell described in FIG. 3 and discussed above, this memory cell of FIG. 4 may be any type of memory cell and will be connected to a column select line as well. Further, in actuality a plurality of memory cells is connected between select line 63 and current drain line 66. This plurality of memory cells is reflected by dotted lines for row select line 63 and current drain line 66.

NPN row driver transistor 69 has an emitter connected to row select line 63, a collector connected to reference voltage line 71, and a base adapted to receive select signal V_s . NPN transistor 72 has its collector connected to reference voltage line 71 and its base adapted to receive select signal V_s . The emitter of transistor 72 is connected to the emitter of PNP transistor 73. Both the base and collector of transistor 73 are connected to the base of PNP transistor 74, one terminal of capacitor 75, and are coupled to the base and collector of NPN transistor 76 by resistors 77, 78, respectively. The emitter of transistor 76 is connected to the other terminal of capacitor 75, the base of PNP transistor 79, and is coupled to ground by current source 81. The collectors of transistors 74, 79 are connected to ground. Transistor 76 and resistors 77, 78 comprise a half cell and will draw a substantially similar current to that of the memory cell comprising transistors 61, 62 and resistors 64, 65. Transistors 73, 79 are matched and will also draw a substantially similar current to each other.

When a negative, or downward transition, select signal V_s is applied to the bases of transistors 69, 72, they will turn off. Current source 81 will pull-down the bases of transistors 73, 74, 79. Transistor 79 will then remove any charge from the memory cell through the standby current drain line 66. Transistor 74 assists by removing any charge appearing on select line 63. Transistors 74, 79 are PNP's and will multiply any current drawn therethrough by beta, thereby improving the rate of discharge.

By now it should be appreciated that there has been provided an improved AC transient driver for memory cells. This transient driver removes inherent stored capacitance charge from the memory cells, without an increased power requirement.

Claims

1. A memory circuit, comprising:

a plurality of memory cells (41, 42, 44, 45, 61, 62, 64, 65) coupled between a selection line (43, 63) and a current drain line (46, 66);

first means (49, 69) responsive to a select signal and coupled to said selection line for providing current to said plurality of memory cells;

a first transistor (52, 72) having a base, an emitter and a collector, said base being responsive to said select signal, said collector being coupled to a first source of operating potential (51, 71);

current supply means (58, 81) for providing a current of predetermined magnitude; characterised by

a second transistor (56, 73) having a base, an emitter and a collector, said base and collector being coupled together to said current supply means;

second means (53, 54, 55, 76, 77, 78) coupled in series with the first and second transistors for conducting substantially the same current as flowing through said plurality of memory cells for the steady state of said select signal which develops a potential thereacross substantially equal to the potential developed across said plurality of memory cells; and

a third transistor (57, 79) having a base, an emitter and a collector, said collector being coupled to a second source of operating potential, said emitter being coupled to said current drain line for sinking current therefrom, said base being coupled to said collector of said second transistor, wherein said current sunk through said third transistor is substantially equal to said current provided by said current supply means for the steady state of said select signal, said current sunk through said third transistor being substantially equal to said current provided by said current supply means multiplied by the beta thereof for the transitions of said select signal.

2. A memory circuit according to claim 1 wherein said second means is coupled between said emitters of said first and second transistors.

3. The memory circuit according to claim 2 wherein said second means includes:

a fourth transistor (53) having an emitter coupled to said emitter of said second transistor and having a base and a collector;

a first resistor (54) coupled between said collector of said fourth transistor and said emitter of said first transistor; and

a second resistor (55) coupled between said base of said fourth transistor and said emitter of said first transistor.

4. The memory circuit according to claim 2 or 3 wherein said first means includes a fifth transistor (49) having a base, an emitter and a collector, said base being responsive to said select signal, said collector being coupled to said first source of operating potential, said emitter being coupled to said selection line.

sets the current level in all devices.

When a negative, or downward transition, select signal V_s is applied to the bases of transistors 49, 52, transistors 49, 52 will turn off. Current source 58 will pull down transistors 56, 57. Transistor 57 will pull down the row memory cells with current I multiplied by β .

Referring to FIG. 4, a second embodiment of the present invention comprises a pair of cross-coupled multi-emitter transistors 61, 62 having their collectors cross-coupled to each others base and coupled to row select line 63 by resistors 64, 65, respectively. A first emitter of each transistor 61, 62 is connected to stand-by current drain line 66. A second emitter of transistor 61 is connected to bit line 67 and a second emitter of transistor 62 is connected to bit line 68. As with the memory cell described in FIG. 3 and discussed above, this memory cell of FIG. 4 may be any type of memory cell and will be connected to a column select line as well. Further, in actuality a plurality of memory cells is connected between select line 63 and current drain line 66. This plurality of memory cells is reflected by dotted lines for row select line 63 and current drain line 66.

NPN row driver transistor 69 has an emitter connected to row select line 63, a collector connected to reference voltage line 71, and a base adapted to receive select signal V_s . NPN transistor 72 has its collector connected to reference voltage line 71 and its base adapted to receive select signal V_s . The emitter of transistor 72 is connected to the emitter of PNP transistor 73. Both the base and collector of transistor 73 are connected to the base of PNP transistor 74, one terminal of capacitor 75, and are coupled to the base and collector of NPN transistor 76 by resistors 77, 78, respectively. The emitter of transistor 76 is connected to the other terminal of capacitor 75, the base of PNP transistor 79, and is coupled to ground by current source 81. The collectors of transistors 74, 79 are connected to ground. Transistor 76 and resistors 77, 78 comprise a half cell and will draw a substantially similar current to that of the memory cell comprising transistors 61, 62 and resistors 64, 65. Transistors 73, 79 are matched and will also draw a substantially similar current to each other.

When a negative, or downward transition, select signal V_s is applied to the bases of transistors 69, 72, they will turn off. Current source 81 will pull-down the bases of transistors 73, 74, 79. Transistor 79 will then remove any charge from the memory cell through the standby current drain line 66. Transistor 74 assists by removing any charge appearing on select line 63. Transistors 74, 79 are PNP's and will multiply any current drawn therethrough by beta, thereby improving the rate of discharge.

By now it should be appreciated that there has been provided an improved AC transient driver for memory cells. This transient driver removes inherent stored capacitance charge from the memory cells, without an increased power requirement.

Claims

1. A memory circuit, comprising:

a plurality of memory cells (41, 42, 44, 45, 61, 62, 64, 65) coupled between a selection line (43, 63) and a current drain line (46, 66);

first means (49, 69) responsive to a select signal and coupled to said selection line for providing current to said plurality of memory cells;

a first transistor (52, 72) having a base, an emitter and a collector, said base being responsive to said select signal, said collector being coupled to a first source of operating potential (51, 71);

current supply means (58, 81) for providing a current of predetermined magnitude; characterised by

a second transistor (56, 73) having a base, an emitter and a collector, said base and collector being coupled together to said current supply means;

second means (53, 54, 55, 76, 77, 78) coupled in series with the first and second transistors for conducting substantially the same current as flowing through said plurality of memory cells for the steady state of said select signal which develops a potential thereacross substantially equal to the potential developed across said plurality of memory cells; and

a third transistor (57, 79) having a base, an emitter and a collector, said collector being coupled to a second source of operating potential, said emitter being coupled to said current drain line for sinking current therefrom, said base being coupled to said collector of said second transistor, wherein said current sunk through said third transistor is substantially equal to said current provided by said current supply means for the steady state of said select signal, said current sunk through said third transistor being substantially equal to said current provided by said current supply means multiplied by the beta thereof for the transitions of said select signal.

2. A memory circuit according to claim 1 wherein said second means is coupled between said emitters of said first and second transistors.

3. The memory circuit according to claim 2 wherein said second means includes:

a fourth transistor (53) having an emitter coupled to said emitter of said second transistor and having a base and a collector;

a first resistor (54) coupled between said collector of said fourth transistor and said emitter of said first transistor; and

a second resistor (55) coupled between said base of said fourth transistor and said emitter of said first transistor.

4. The memory circuit according to claim 2 or 3 wherein said first means includes a fifth transistor (49) having a base, an emitter and a collector, said base being responsive to said select signal, said collector being coupled to said first source of operating potential, said emitter being coupled to said selection line.



5. A memory circuit according to claim 1 wherein said emitter of said second transistor is coupled to said emitter of said first transistor, said second means is coupled between the collector of said second transistor and said current supply means, and said memory circuit further comprises a fourth transistor (74) having a base, an emitter and a collector, said collector being coupled to said second source of operating potential, said emitter being coupled to said selection line for sinking the current therefrom, said base being coupled to said collector and base of said second transistor.

6. A memory circuit according to claim 5 wherein said second means comprises:

a fifth transistor (76) having a base, a collector and an emitter coupled to said current supply means;

a first resistor (77) coupled between said base of said fifth transistor and said collector of said second transistor; and

a second resistor (78) coupled between said collector of said fifth transistor and said collector of said second transistor.

7. A memory circuit according to claim 6 wherein said second means further includes capacitive means (75) coupled between said base of said second transistor and said base of said third transistor.

8. A memory circuit according to claim 6 or 7 wherein said first means includes a sixth transistor (69) having a base, an emitter and a collector, said base being responsive to said select signal, said collector being coupled to said first source of operating potential, said emitter being coupled to said selection line.

9. A memory circuit according to any preceding claim wherein a memory cell includes:

a first transistor (41, 61) having a base, first and second emitters and a collector, said first emitter being coupled to a first terminal at which a third potential is applied, said second emitter being coupled to said current drain line;

a second transistor (42, 62) having a base, first and second emitters and a collector, said first emitter being coupled to a second terminal at which a fourth potential is applied, said second emitter being coupled to said current drain line, said base of said second transistor being coupled to said collector of said first transistor, said collector of said second transistor being coupled to said base of said first transistor;

first resistor (44, 64) coupled between said collector of said first transistor and said selection line; and

second resistor (45, 65) coupled between said collector of said second transistor and said selection line.

Patentansprüche

1. Speicherschaltung

mit mehreren Speicherzellen (41, 42, 44, 45, 61, 62, 64, 65), die zwischen einer Wahlleitung (43, 63) und einer Stromzugleitung (46, 66) angeschlossen sind,

mit einer ersten an der Wahlleitung angeschlossenen Vorrichtung (49, 69), die auf ein Wahlsignal anspricht, um die Speicherzellen mit Strom zu versorgen,

mit einem ersten eine Basis, einen Emmitter und einen Kollektor aufweisenden und auf das Wahlsignal ansprechenden Transistor (52, 72), wobei der Kollektor an eine erste Betriebspotentialquelle (51, 71) angeschlossen ist,

und mit einer Stromquelle (58, 81) zur Lieferung eines Stromes von vorherbestimmter Stärke, gekennzeichnet

durch einen zweiten eine Basis, einen Emmitter und einen Kollektor aufweisenden Transistor (56, 73), wobei die Basis und der Kollektor an der Stromquelle zusammengeschlossen sind,

durch eine zweite mit dem ersten und zweiten Transistor in Reihe liegende Vorrichtung (53, 54, 55, 76, 77, 78) zur Führung im wesentlichen desselben Stromes wie desjenigen, der durch die Speicherzellen im stetigen Zustand des Wahlsignals fließt, das an ihr ein Potential entwickelt, das mit dem Potential nahezu übereinstimmt, das an den Speicherzellen entwickelt wird, und

durch einen dritten eine Basis, einen Emmitter und einen Kollektor aufweisenden Transistor (57, 79), wobei der Kollektor an der zweiten Betriebsspannungsquelle, der Emmitter an der Stromzugleitung zur Absenkung des von ihr geführten Stromes und die Basis an dem Kollektor des zweiten Transistors angeschlossen sind, wobei der durch den dritten Transistor herabgesetzte Strom im wesentlichen gleich dem Strom ist, der für den stetigen Zustand des Wahlsignals von der Stromquelle geliefert wird, und der durch den dritten Transistor herabgesetzte Strom im wesentlichen gleich dem Strom ist, der für die Übergänge des Wahlsignals von der Stromquelle, multipliziert mit β , geliefert wird.

2. Speicherschaltung gemäß Anspruch 1, bei dem die zweite Vorrichtung zwischen den Emittern des ersten und zweiten Transistors angeschlossen ist.

3. Speicherschaltung gemäß Anspruch 2, bei der zur zweiten Vorrichtung gehören:

ein vierter Transistor (53), dessen Emmitter an dem Emmitter des zweiten Transistors angeschlossen ist, und der eine Basis und einen Kollektor aufweist,

ein erster Widerstand (54), der zwischen dem Kollektor des vierten Transistors und dem Emmitter des ersten Transistors angeschlossen ist, und

ein zweiter Widerstand (55), der zwischen der Basis des vierten Transistors und dem Emmitter des ersten Transistors angeschlossen ist.

4. Speicherschaltung gemäß Anspruch 2 oder 3, bei der die erste Vorrichtung einen fünften eine Basis, einen Emmitter und einen Kollektor aufweisenden Transistor (49) enthält, bei dem seine Basis auf das Wahlsignal anspricht und sein Kollektor an der ersten Betriebspotentialquelle und sein Emmitter an der Wahlleitung angeschlossen ist.

5. Speicherschaltung gemäß Anspruch 1, bei der der Emmitter des zweiten Transistors an dem Emmitter des ersten Transistors und die zweite Vorrichtung zwischen dem Kollektor des zweiten Transi-



stors und der Stromquelle angeschlossen ist, und bei der ferner ein vierter mit einer Basis, einem Emittter und einem Kollektor versehener Transistor (74) mit seinem Kollektor an der zweiten Betriebspotentialquelle, mit seinem Emittter an der Wahlleitung zur Herabsetzung des daraus austretenden Stromes und mit seiner Basis an dem Kollektor und der Basis des zweiten Transistors angeschlossen ist.

6. Speicherschaltung gemäß Anspruch 5, bei der zu der zweiten Vorrichtung gehören:

ein fünfter an der Stromquelle angeschlossener Transistor (76), der eine Basis, einen Kollektor und einen Emittter besitzt,

ein erster Widerstand (77), der zwischen der Basis des fünften Transistors und dem Kollektor des zweiten Transistors angeschlossen ist, und

ein zweiter Widerstand (78), der zwischen dem Kollektor des fünften Transistors und dem Kollektor des zweiten Transistors angeschlossen ist.

7. Speicherschaltung gemäß Anspruch 6, bei der die zweite Vorrichtung eine Kapazität (75) enthält, die zwischen der Basis des zweiten Transistors und der Basis des dritten Transistors angeschlossen ist.

8. Speicherschaltung gemäß Anspruch 6 oder 7, bei der die erste Vorrichtung einen sechsten eine Basis, einen Emittter und einen Kollektor aufweisenden Transistor (69) enthält, bei dem die Basis auf das Wahlsignal anspricht und der Kollektor an die erste Betriebspotentialquelle und der Emittter an die Wahlleitung angeschlossen ist.

9. Speicherschaltung gemäß einem vorhergehenden Anspruch, bei der zu einer Speicherzelle gehören:

ein erster Transistor (41, 61) mit einer Basis, zwei Emitttern und einem Kollektor, wobei der erste Emittter an einer ersten Klemme liegt, an der ein drittes Potential angelegt ist, und der zweite Emittter mit der Stromzugleitung verbunden ist,

ein zweiter Transistor (42, 62) mit einer Basis, zwei Emitttern und einem Kollektor, wobei der erste Emittter an einer zweiten Klemme liegt, an der ein viertes Potential angelegt ist, und der zweite Emittter mit der Stromzugleitung, die Basis des zweiten Transistors mit dem Kollektor des ersten Transistors und der Kollektor des zweiten Transistors mit der Basis des ersten Transistors verbunden ist,

ein erster Widerstand (44, 64), der zwischen dem Kollektor des ersten Transistors und der Wahlleitung angeschlossen ist, und

ein zweiter Widerstand (45, 65), der zwischen dem Kollektor des zweiten Transistors und der Wahlleitung angeschlossen ist.

Revendications

1. Circuit mémoire comprenant:

une pluralité de cellules mémoire (41, 42, 44, 45, 61, 62, 64, 65) couplées entre une ligne de sélection (43, 63) et une ligne de retour de courant (46, 66);

un premier moyen (49, 59) sensible à un signal de sélection et couplé à la ligne de sélection pour

fournir un courant à la pluralité de cellules mémoire;

un premier transistor (52, 72) comportant une base, un émetteur et un collecteur, la base étant sensible au signal de sélection, le collecteur étant couplé à une première source de potentiel de fonctionnement (51, 71);

un moyen d'alimentation en courant (58, 81) pour fournir un courant d'une amplitude prédéterminée; caractérisé par:

un second transistor (56, 73) comportant une base, un émetteur et un collecteur, la base et le collecteur étant couplés ensemble au moyen d'alimentation en courant;

un second moyen (53, 54, 55, 76, 77, 78) couplé en série avec les premier et second transistors pour conduire sensiblement le même courant que celui qui traverse la pluralité de cellules mémoire pour l'état d'attente du signal de sélection qui développe un potentiel sensiblement égal au potentiel développé pour la pluralité de cellules mémoire, et

un troisième transistor (57, 79) comportant une base, un émetteur et un collecteur, le collecteur étant couplé à une seconde source de potentiel de fonctionnement, l'émetteur étant couplé à la ligne de retour de courant pour abaisser le courant qui circule, la base étant couplée au collecteur du second transistor, dans lequel le courant abaissé qui traverse le troisième transistor est sensiblement égal au courant fourni par le moyen d'alimentation en courant pour l'état d'attente du signal de sélection, le courant abaissé qui traverse le troisième transistor étant sensiblement égal au courant fourni par le moyen d'alimentation en courant multiplié par le gain beta de celui-ci pour les transitions du signal de sélection.

2. Circuit mémoire selon la revendication 1, dans lequel le second moyen est couplé entre les émetteurs des premier et seconds transistors.

3. Circuit mémoire selon la revendication 2, dans lequel le second moyen comporte:

un quatrième transistor (53) comportant un émetteur couplé à l'émetteur du second transistor et comportant une base et un collecteur;

une première résistance (54) couplée entre le collecteur du quatrième transistor et l'émetteur du premier transistor; et

une seconde résistance (55) couplée entre la base du quatrième transistor et l'émetteur du premier transistor.

4. Circuit mémoire selon la revendication 2 ou 3, dans lequel le premier moyen comporte un cinquième transistor (59) qui comporte une base, un émetteur et un collecteur, la base étant sensible au signal de sélection, le collecteur étant couplé à la première source de potentiel de fonctionnement, l'émetteur étant couplé à la ligne de sélection.

5. Circuit mémoire selon la revendication 1, dans lequel l'émetteur du second transistor est couplé à l'émetteur du premier transistor; le second moyen est couplé entre le collecteur du second transistor et le moyen d'alimentation en courant, et en ce que le circuit mémoire com-



prend en outre un quatrième transistor (74) qui comporte une base, un émetteur et un collecteur, le collecteur étant couplé à la seconde source de potentiel de fonctionnement, l'émetteur étant couplé à la ligne de sélection pour abaisser le courant qui la traverse, la base étant couplée au collecteur et à la base du second transistor.

6. Circuit mémoire selon la revendication 5, dans lequel le second moyen comprend:

un cinquième transistor (76) comportant une base, un collecteur et un émetteur couplé au moyen d'alimentation en courant;

une première résistance (77) couplée entre la base du cinquième transistor et le collecteur du second transistor; et

une seconde résistance (78) couplée entre le collecteur du cinquième transistor et le collecteur du second transistor.

7. Circuit mémoire selon la revendication 6, dans lequel le second moyen comprend en outre un moyen de capacité (75) couplé entre la base du second transistor et la base du troisième transistor.

8. Circuit mémoire selon la revendication 6 ou 7, dans lequel le premier moyen comporte un sixième transistor (69) comportant une base, un émetteur et un collecteur, la base étant sensible au signal de sélection, le collecteur étant couplé à

la première source de potentiel de fonctionnement, l'émetteur étant couplé à la ligne de sélection.

5 9. Circuit mémoire selon l'une quelconque des revendications qui précèdent, dans lequel une cellule mémoire comporte:

10 un premier transistor (41, 61) comportant une base, des premier et second émetteurs et un collecteur, le premier émetteur étant couplé à une première borne au niveau de laquelle un troisième potentiel est appliqué, le second émetteur étant couplé à la ligne de retour de courant;

15 un second transistor (42, 62) comportant une base, des premier et second émetteurs et un collecteur, le premier émetteur étant couplé à une seconde borne au niveau de laquelle un quatrième potentiel est appliqué, le second émetteur étant couplé à la ligne de retour de courant, la base du second transistor étant couplée au collecteur du premier transistor, le collecteur du second transistor étant couplé à la base du premier transistor;

20 une première résistance (44, 64) couplée entre le collecteur du premier transistor et la ligne de sélection; et

25 une seconde résistance (45, 65) couplée entre le collecteur du second transistor et la ligne de sélection.

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