2067332

33

"IMPROVEMENTS IN OR RELATING TO ELECTRO-OPTICAL DISPLAY ARRANGEMENTS"

This invention relates to electro-optical display arrangements, and more particularly, though not exclusively, to electro-optical display arrangements employing, for providing a display, phase transition mode liquid crystal display devices.

In twisted nematic liquid crystal display devices, LED display devices and similar electro-optical display devices, predetermined voltages - for example of about 3 volts - are applied to selected picture elements in the display and zero voltage is applied to non-selected picture elements therein. However, in certain electro-optical display devices such as phase transition mode liquid crystal display devices, desired voltages other than zero may be applied to non-selected picture elements in the display while other predetermined voltages are applied to the selected elements. A phase transition mode liquid crystal display element may take any of three phases or states, i.e., a homeo-tropic state, (hereinafter called the H-state), a focal-conic state (hereinafter called the F-state), and a granjuane state (hereinafter called the G-state), depending on the applied voltage. The G-state is a transparent state occurring in the condition of no applied electric field. This state is changed into the F-state - which is a light scattering state - when a voltage of appropriate value is applied. This state is changed into the H-state - a transparent state - when an appropriate higher voltage is applied. It is possible to make use of the transparent G-state and the light scattering F-state to achieve display. In a

display arrangement operating in this way, a static driving method similar to that commonly used for driving an ordinary twisted nematic mode liquid crystal display device may be employed by applying a square wave voltage having an effective value ($\pm V_F$) such as to hold the liquid crystal in the F-state, between selected display segment electrodes and a common electrode and applying zero volts between non-selected display segment electrodes and said common electrode. However, it takes a very considerable time to achieve at a picture element a full transition from the F-state to the G-state so that there is apt to be inferior transparency in the G-state.

Digital integrated circuits are commonly used for driving liquid crystal display arrangements, in order to minimise power consumption and occupation of available space, which is often very limited indeed. When digital integrated circuits are used as driving circuits the voltage level required for driving the liquid crystal may be obtained by boosting or by using condensers to drop the voltage from a source of voltage supply, and accordingly the voltage level which can be attained in practice is limited to integral times or to integral fractions of the voltage from a power source, e.g., the voltage from a battery. However, because of the electric properties of a phase transition mode liquid crystal, the voltage for producing the F-state or the H-state is not equivalent to the voltage level obtained by boosting or by dropping a supply source voltage. The picture quality - the contrast - in

a displayed picture produced by a phase transition mode liquid crystal device depends on the applied effective voltage.

The foregoing considerations render it very difficult in practice to achieve, with a desirably low consumption of power, satisfactory picture displays of good quality and quick response from electro-optical display devices such as phase transition mode liquid crystal devices and the present invention seeks to overcome these difficulties and to provide arrangements of a quick response low power consumption and involving the use of relatively simple, easily manufactured and reliable driving circuits.

According to this invention a display arrangement includes a display device with an electro-optical display body sandwiched between display electrodes and a common electrode; and, for driving said device, a driving circuit comprising means for applying at selected and non-selected display picture elements in said device two square voltage waves having effective voltages other than zero volts and at least one of which has intervals of zero volts level and means for independently setting the zero volts level intervals in at least one of said waves. It should be noted here that the term square waves as employed in this specification and claims, is used in its customary sense to include wave forms which, more strictly and pedantically speaking, would be termed rectangular.

Preferably each of said square voltage waves has intervals of zero volts level. In this case provision is preferably made for independently setting the zero volts level intervals in each of the

two waves independently.

Preferably the electro-optical display device is a phase transition mode liquid crystal device and the states of the phase transition mode liquid crystal utilised for achieving a display may be the focal-conic state and the homeotropic state.

In one way of carrying out the invention there is provided a display arrangement comprising a display device having a phase transition mode liquid crystal body sandwiched between display electrodes and common electrode, and in a driving circuit for driving said device, means for generating and applying to the device two square voltage waves, one of which has an effective voltage such as will impart a homeotropic state to said liquid crystal body and has desired intervals of zero volts level, and the other of which has an effective voltage such as will impart a focal-conic state to said liquid crystal body and has desired intervals of zero volts level.

The invention is illustrated in and further explained in connection with the accompanying drawings in which:-

Fig. 1 is a simplified block diagram of a preferred embodiment of the invention;

Fig. 2 is a waveform diagram of voltage applied to the common electrode of a display device;

Fig. 3 is a waveform diagram of voltage applied to selected segment electrodes of a display device;

Fig. 4 is a waveform diagram of voltage applied to non-selected segment electrodes of a display device;

Fig. 5 is a waveform diagram of voltage between the common electrode and selected segment electrodes of a display device;

Fig. 6 is a waveform diagram of voltage between the common electrode and non-selected segment electrodes of a display device;

Fig. 7 is a circuit diagram showing, so far as is necessary to an understanding thereof, a driving voltage generating circuit, for generating control signals to produce first, second and third driving voltage waves;

Fig. 8 is a waveform diagram of voltage at the input terminal 14 in Fig. 7;

Fig. 9 is a waveform diagram of voltage at the output terminal 11 in Fig. 7;

Fig. 10 is a waveform diagram of voltage at the output terminal 10 in Fig. 7;

Fig. 11 is a waveform diagram of voltage at the output terminal 13 in Fig. 7;

Fig. 12 is a waveform diagram of voltage at the output terminal 12 in Fig. 7; and

Fig. 13 is a circuit diagram showing, so far as is necessary to an understanding thereof, a driving voltage generating circuit for selecting and composing voltage levels under the control of control signals.

Referring to Fig. 1, block 1 represents a generating circuit for generating a constant clock signal which is supplied to a control signal circuit 2 and to a driving voltage generating circuit 3. The control signal circuit 2 produces control signals in synchronism with clock signals derived from circuit 1, said control signal circuit 2 producing information signals which are used to determine the segment electrodes to be selected or non-

39

selected and the times at which such selection or non-selection is to be effected. These information signals from circuit 2 are applied to and control the operation of a segment electrode driving circuit 4. The driving voltage generating circuit 3 produces three driving voltage waves two of which are square and are passed to the segment electrode driving circuit 4 and the remaining one of which is fed to the common electrode of a display cell which is represented by the block 5.

The first of the foregoing three voltage waves is represented in Figure 2. It is a square wave $(0,V_N)$ having an amplitude of $V_N/2$ and 1/2 duty ratio, and is continuously applied to the common electrode of the display cell 5. The second square voltage wave is represented in Figure 3. It is a wave $(V_N,0)$ having an amplitude of $V_N/2$, and 1/2 duty ratio and is phase shifted by a time τ_1 (within a half period of the first wave) with respect to a voltage wave 180° out of phase with the first wave. The third voltage wave is represented in Figure 4. It takes the following four voltage level periodically, namely, V_M, V_N, V_N-V_M and 0, as shown in Figure 4. The level "V_M" exists during the interval "$T-\tau_2$" occurring after the level of the first wave takes the value "V_N". "T" is the time occupied by a half period of the first wave (Figure 2) and the phase relation τ_2 (Figure 4) is chosen to satisfy relations $0<\tau_2<T$. The level "V_N" appears for an interval "τ_2". When the level of the first wave is zero volts, the level "V_N-V_M" appears for an interval "$T-\tau_2$" and after that

the level "O" appears for a remaining interval "τ_2". The relation between the voltage levels V_M, V_N, an effective value V_O (giving a selected state to an electro-optical display element, e.g., the H-state in a phase transition mode liquid crystal), and an effective value V_1, (giving a non-selected state, e.g. the F-state) is represented by the following relations,

$$V_1 < V_M < V_N \ , \ V_N > V_O.$$

The second and third square voltage waves are selected by the segment electrode driving circuit 4 under the control of the control signals from 2 and are applied to the appropriate display electrodes of the display cell 5.

Fig. 5 shows the voltage waveform produced between display electrodes in the selected state and the common electrode. It is a square voltage wave $\pm V_N$, having an amplitude of V_N with a time interval "τ_1" of zero volts level.

Fig. 6 shows the voltage waveform produced between display electrodes in the non-selected state and the common electrode. It is a square voltage wave $\pm V_M$, having an amplitude of V_M and a time interval "τ_2" of zero volts level.

The effective value of the voltage applied to a display element is given by:-

Effective value:

$$\left\{\frac{1}{2T}\int_0^{2T} V^2(t)dt\right\}^{\frac{1}{2}}$$

The effective voltage in the selected state is given by:-

41

$$\left[\frac{1}{2T}\left\{\int_0^{T-\tau_1} (V_N)^2\, dt + \int_T^{2T-\tau_1} (-V_N)^2\, dt\right\}\right]^{\frac{1}{2}}$$

$$= \left[\frac{1}{2T}\left\{V_N^2\ (T-\tau_1) + V_N^2\ (2T-\tau_1-T)\right\}\right]^{\frac{1}{2}}$$

$$= V_N\left(1-\frac{\tau_1}{T}\right)^{\frac{1}{2}}$$

The effective voltage in the selected state is equal to the voltage V_O wherein:-

$$V_O = V_N\left(1-\frac{\tau_1}{T}\right)^{\frac{1}{2}}$$

The effective voltage in the non-selected state is given by:-

$$\left[\frac{1}{2T}\left\{\int_0^{T-\tau_2} (V_M)^2\, dt + \int_T^{2T-\tau_2} (-V_M)^2\, dt\right\}\right]^{\frac{1}{2}}$$

$$= \left[\frac{1}{2T}\left\{V_M^2(T-\tau_2) + V_M^2\ (2T-\tau_2-T)\right\}\right]^{\frac{1}{2}}$$

$$= V_M\left(1-\frac{\tau_2}{T}\right)^{\frac{1}{2}}$$

The effective voltage in the non-selected state is equal

to the voltage V_1 whence:-

42

$$V_1 = V_M(1- \frac{\tau_2}{T})^{\frac{1}{2}}$$

The values of "τ_1" and the "τ_2" may be determined independently and are so chosen that the effective values in the selected and non-selected states are equal to the voltages V_0 and V_1 respectively. Consequently, it is possible to achieve highly satisfactory driving of an electro-optical display device such as a phase transition mode liquid crystal device utilizing the F-state and the H-state to obtain a display, and to attach a desirably short response time and desirably good contrast in the resulting picture.

Because the voltage waves applied between the display segment electrodes and the common electrode are of zero volts during the intervals τ_1 and τ_2, the electric charge collected between the display segment electrodes and the common electrode can be readily and quickly discharged. This fact contributes greatly to the attainment of a low power consumption and consequent long useful life for the power source.

Fig. 7 shows that part of a preferred form of driving voltage generating circuit 3 for producing at terminals 10, 11, 12 and 13 control signals for obtaining the aforesaid third square voltage wave.

Referring to Fig. 7, an input signal, hereinafter termed the A signal is applied at terminal 14. This A signal is in phase with the aforesaid first square voltage wave and oscillates

43

between 0 volts and the power source voltage V_C of a digital IC (integrated circuit), as shown in Fig. 8. An input signal, hereinafter called the B signal, is applied to terminal 15. The B signal, which is a clock signal produced by the clock signal generating circuit 1 or derived therefrom by frequency division, is a square voltage wave oscillating between 0 volts and the power source voltage V_C.

A pulse of half the wavelength of the B signal is produced by a D-flipflop 6a and an AND gate 7a at the time of the leading edge of the A signal, and is fed to the set terminal of an R-S flipflop 16a and to the reset terminal of a counter 8a thereby to set the said R-S flipflop 16a and to reset the said counter 8a.

Similarly, a pulse of half the wavelength of the B signal is produced by a D-flipflop 6b and an AND gate 7b at the time of the leading edge of a signal which is 180° out of phase with the A signal, and is fed to the set terminal of an R-S flipflop 16b and to the reset terminal of a counter 8b thereby to set the said R-S flipflop 16b and to reset the said counter 8b.

Upon being reset, the counters 8a and 8b start counting at the time of the next leading edge of the B signal.

When the counts in the counters 8a, 8b are coincident with a desired binary value which can be set by switches 17, a pulse of half the wavelength of the B signal is produced at the output terminals of NOR gates 9a, 9b and fed to the reset terminals of the R-S flipflops 16a and 16b and these R-S flipflops are reset.

The outputs from the R-S flip-flops 16a and 16b, which appear at the terminals 11 and 13 are as shown in Figures 9 and 11 respectively.

The output of the R-S flip-flop 16a inverted by an inverter and the A signal are fed to the respective inputs of an AND gate, and a signal as shown in Figure 10 is produced at the terminal 10. Also the output of the R-S flip-flop 16b is inverted, the A signal is inverted, and these inverted signals are applied to the inputs of an AND gate, so that a signal as shown in Figure 12 is produced at the terminal 12.

The four outputs at the terminals 10, 11, 12 and 13 are applied respectively to the terminals referenced 10', 11', 12' and 13' of the circuit shown in Figure 13. In Figure 13, the voltage levels V_N, V_M, $V_N - V_M$ and 0 volts are selected and composed analogically by transmission gates 18e, 18f, 18g and 18h in accordance with the said four outputs, producing at the terminal 21, the aforesaid third square voltage wave as shown in Figure 3.

The A signal and the B signal are fed to input terminals 14' and 15' respectively, in Figure 13.

The voltages V_N and 0 volts are selected and composed in transmission gates 18a, 18b by the A signal and the said A signal inverted, and there is produced at the terminal 19 an output which constitutes the aforesaid first square voltage wave.

The three D-flip-flops 22a, 22b, 22c serve to produce a signal, hereinafter called the C signal, having a desired phase

shift with respect to the A signal. The voltages 0 volts and V_N are selected and composed in transmission gates 18c, 18d by the C signal and the said C signal inverted, so that there is produced at the terminal 20, the aforesaid second square voltage wave.

It should be noted that the application of the invention is not limited to arrangements employing phase transition mode liquid crystal display devices but is of more general application and may be applied to other arrangement employing a display device requiring, for its operation, the application of voltages other than zero volts for both selected and non-selected display picture elements.

CLAIMS

1. A display arrangement including a display device with an electro-optical display body sandwiched between display electrodes and a common electrode; and, for driving said device, a driving circuit comprising means for applying at selected and non-selected display picture elements in said device two square voltage waves having effective voltages other than zero volts and at least one of which has intervals of zero volts level and means for independently setting the zero volts level intervals in at least one of said waves.

2. An arrangement as claimed in claim 1 wherein each of said square voltage waves has intervals of zero volts level.

3. An arrangement as claimed in claim 2 and including provision for independently setting the zero volts level intervals in each of the two waves independently.

4. An arrangement as claimed in any of the preceding claims wherein the electro-optical display device is a phase transition mode liquid crystal device.

5. An arrangement as claimed in claim 4 wherein the states of the phase transition mode liquid crystal utilized for achieving a display are the focal-conic state and the homeotropic state.

6. A display arrangement comprising a display device having a phase transition mode liquid crystal body sandwiched between

display electrodes and common electrode, and in a driving circuit for driving said device, means for generating and applying to the device two square voltage waves, one of which has an effective voltage such as will impart a homeotropic state to said liquid crystal body and has desired intervals of zero volts level, and the other of which has an effective voltage such as will impart a focal-conic state to said liquid crystal body and has desired intervals of zero volts level.

7. An arrangement as claimed in any of the preceding claims and comprising a driving circuit including square wave generating means substantially as herein described with reference to Figures 7 and 13 of the accompanying drawings.

8. Display arrangements substantially as herein described with reference to the accompanying drawings.

The text of the specification has been reproduced by photocopying the applicants original typescript. It may contain a few amendments which are difficult to read. The original typescript containing these amendments may be inspected on the premises of the Patent Office

ERRATUM

SPECIFICATION NO 2067332B

Front page, Heading (73) Proprietor *for* Daini Seikosha KK *read* Kabushiki Kaisha Daini Seikosha

THE PATENT OFFICE
17 August 1983

Bas 253451/13

(25)

ERRATUM

SPECIFICATION NO 2067332B

Front page, Heading (73) Proprietor *for* Daini Seikosha KK *read* Kabushiki Kaisha Daini Seikosha

THE PATENT OFFICE
17 August 1983

Bas 253451/13