CLAIMS

1. A high-voltage nitride device, comprising:

a silicon substrate;

a nitride epitaxial layer, prepared on the silicon substrate;

a source electrode and a drain electrode, both of which are contacted with the nitride epitaxial layer;

a gate electrode, prepared between the source electrode and the drain electrode;

at least one etched hole, formed in the nitride epitaxial layer; and,

at least one spatial isolation area, formed in a region between the silicon substrate and the nitride epitaxial layer vertically and between the source electrode and the drain electrode horizontally by implementing an etching/corrosion process respectively in the at least one etched hole laterally.

2. The device of Claim 1, wherein the at least one spatial isolation area is formed in a region between the silicon substrate and the nitride epitaxial layer vertically and between the gate electrode and the drain electrode horizontally.

3. The device of Claim 1, wherein the nitride epitaxial layer comprises:

a nitride nucleation layer prepared on the silicon substrate;

a nitride buffer layer prepared on the nitride nucleation layer; and

preparing a source electrode and a drain electrode on the nitride epitaxial layer; both of which are contacted with the nitride epitaxial layer;

preparing a gate electrode between the source electrode and the drain electrode;

forming at least one etched hole in the nitride epitaxial layer; and

forming at least one spatial isolation area in a region between the silicon substrate and the nitride epitaxial layer vertically and between the source electrode and the drain electrode horizontally by implementing an etching/corrosion process respectively in the at least one etched hole laterally.

18. The method of Claim 17, wherein preparing a nitride epitaxial layer on a silicon substrate provided comprises:

preparing a nitride nucleation layer prepared on the silicon substrate;

preparing a nitride buffer layer prepared on the nitride nucleation layer;

preparing a nitride channel layer prepared on the nitride buffer layer.

~~19. The method of Claim 17, wherein forming at least one spatial isolation area in a region between the silicon substrate and the nitride epitaxial layer vertically and between the source electrode and the drain electrode horizontally comprises:~~

~~implementing a dry etching process and/or a wet corroding process to form the at least one spatial isolation area.~~

~~20~~19. The method of Claim 17, wherein ~~forming at least one spatial isolation area in a region between the silicon substrate and the nitride epitaxial~~

~~layer vertically and between the source electrode and the drain electrode horizontally~~forming at least one etched hole in the nitride epitaxial layer comprises:

forming at least one etched hole, which is located in the nitride epitaxial layer and between the drain electrode and the gate electrode horizontally; and/or,

forming at least one etched hole, which is located in the nitride epitaxial layer outside of the drain electrode horizontally; and/or,

forming at least one etched hole, which is located in the nitride epitaxial layer and between the source electrode and the gate electrode horizontally; and/or,

forming at least one etched hole, which is located in the nitride epitaxial layer outside of the source electrode horizontally~~; and,~~

~~implementing an etching process and/or a wet corrosion process in the at least one etched hole laterally~~.