

APPARATUS AND MANUFACTURING METHOD

[0001] This application claims priority to Chinese Patent Application No. 201510535388.X, filed with the Chinese Patent Office on August 27, 2015 and entitled "APPARATUS AND MANUFACTURING METHOD", which is incorporated herein by reference in its entirety.

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TECHNICAL FIELD

[0002] The present invention relates to the circuit field, and in particular, to a circuit apparatus and a manufacturing method.

BACKGROUND

[0003] FIG. 1A is a schematic sectional view of an integrated circuit chip in the prior art and a partial packaging structure of the integrated circuit chip. The structure includes an integrated circuit chip 1A02, a thermal interface material layer 1A04, and a heat sink device 1A06. Heat generated by the integrated circuit chip 1A02 in an operating process is dissipated to the heat sink device 1A06 by using the thermal interface material layer 1A04 on a rear surface of the chip. Therefore, a heat conduction capability of the thermal interface material layer 1A04 significantly affects heat dissipation of the chip. An existing thermal interface material layer includes a silver adhesive material. Metal silver particles 1A08 are mixed in the silver adhesive material to improve an effect of heat conduction, but the effect of heat conduction mainly depends on continuous phases formed by the silver adhesive material. The silver adhesive material has a low thermal conductivity, and can hardly satisfy a heat dissipation requirement of a high-power chip.

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SUMMARY

[0004] Embodiments of the present invention provide an apparatus and a manufacturing method. In the apparatus, a thermal interface material between a circuit device and a heat sink fin has a relatively high thermal conductivity, greatly improves heat conduction efficiency of an entire heat path, and can better satisfy a heat dissipation requirement of a circuit device having high power consumption.

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[0005] According to a first aspect, an embodiment of the present invention provides an

apparatus, including: a circuit device; a heat sink fin; and a thermal interface material layer, thermally coupled to the circuit device and the heat sink fin, and including: a first alloy layer, thermally coupled to the circuit device; a nanometal particle layer, thermally coupled to the first alloy layer, where the nanometal particle layer includes multiple nanometal particles that are coupled to each other and an intermediate mixture, and the intermediate mixture is filled between the multiple nanometal particles; and a second alloy layer, thermally coupled to the nanometal particle layer and the heat sink fin.

[0006] In a first possible implementation manner of the first aspect, a sintered continuous phase structure is formed at a contact portion between the first alloy layer and the nanometal particle layer, sintered continuous phase structures are formed at contact portions between the multiple nanometal particles, and a sintered continuous phase structure is formed at a contact portion between the second alloy layer and the nanometal particle layer.

[0007] With reference to the first aspect or the first possible implementation manner of the first aspect, in a second possible implementation manner, the nanometal particles include silver.

[0008] With reference to any one of the first aspect, or the first to the second possible implementation manners of the first aspect, in a third possible implementation manner, diameters of the nanometal particles are between 50 nanometers and 200 nanometers.

[0009] With reference to any one of the first aspect, or the first to the third possible implementation manners of the first aspect, in a fourth possible implementation manner, the apparatus is applied to a flip chip ball grid array structure.

[0010] With reference to any one of the first aspect, or the first to the fourth possible implementation manners of the first aspect, in a fifth possible implementation manner, the first alloy layer includes a first adhesive layer and a first co-sintered layer, the first adhesive layer is thermally coupled to the circuit device, the first co-sintered layer is coupled to the nanometal particle layer, and a sintered continuous phase structure is formed at a contact portion between the first co-sintered layer and the nanometal particle layer.

[0011] With reference to the fifth possible implementation manner of the first aspect, in a sixth possible implementation manner, the first adhesive layer includes any one of the following materials: titanium, chromium, nickel, or a nickel-vanadium alloy, and the first co-sintered layer includes any one of the following materials: silver, gold, or copper.

[0012] With reference to either of the fifth possible implementation manner and the sixth possible implementation manner of the first aspect, in a seventh possible implementation manner, the first alloy layer further includes a first buffer layer located between the first adhesive layer and the first co-sintered layer, and the first buffer layer includes any one of the following materials:

aluminum, copper, nickel, or a nickel-vanadium alloy.

[0013] With reference to any one of the first aspect, or the first to the seventh possible implementation manners of the first aspect, in an eighth possible implementation manner, the second alloy layer includes a second adhesive layer and a second co-sintered layer, the second adhesive layer is thermally coupled to the heat sink fin, the second co-sintered layer is thermally coupled to the nanometal particle layer, and a sintered continuous phase structure is formed at a contact portion between the second co-sintered layer and the nanometal particle layer.

[0014] With reference to the eighth possible implementation manner of the first aspect, in a ninth possible implementation manner, the second adhesive layer includes any one of the following materials: titanium, chromium, nickel, or a nickel-vanadium alloy, and the second co-sintered layer includes any one of the following materials: silver, gold, or copper.

[0015] With reference to either of the eighth possible implementation manner and the ninth possible implementation manner of the first aspect, in a tenth possible implementation manner, the second alloy layer further includes a second buffer layer located between the second adhesive layer and the second co-sintered layer, and the second buffer layer includes any one of the following materials: aluminum, copper, nickel, or a nickel-vanadium alloy.

[0016] With reference to any one of the first aspect, or the first to the tenth possible implementation manners of the first aspect, in an eleventh possible implementation manner, diameters of the nanometal particles are not greater than 1 micrometer.

[0017] With reference to any one of the first aspect, or the first to the eleventh possible implementation manners of the first aspect, in a twelfth possible implementation manner, the intermediate mixture includes any one of the following materials: air or resin.

[0018] With reference to any one of the first aspect, or the first to the twelfth possible implementation manners of the first aspect, in a thirteenth possible implementation manner, the circuit device includes an integrated circuit die, and a substrate of the integrated circuit die is thermally coupled to thermal interface material layer.

[0019] According to a second aspect, an embodiment of the present invention provides a method for manufacturing an apparatus, including: generating a first alloy layer; generating a nanometal particle layer by using multiple nanometal particles that are coupled to each other and an intermediate mixture, and filling the intermediate mixture between the multiple nanometal particles; and generating a second alloy layer, thermally coupling the first alloy layer to the circuit device, thermally coupling the nanometal particle layer to the first alloy layer, and thermally coupling the second alloy layer to the nanometal particle layer and the heat sink fin.

[0020] In a first possible implementation manner of the second aspect, the method further

includes: forming a sintered continuous phase structure at a contact portion between the first alloy layer and the nanometal particle layer, forming sintered continuous phase structures at contact portions between the nanometal particles, and forming a sintered continuous phase structure at a contact portion between the second alloy layer and the nanometal particle layer.

5 **[0021]** With reference to the second aspect or the first possible implementation manner of the second aspect, in a second possible implementation manner, diameters of the nanometal particles are not greater than 1 micrometer.

10 **[0022]** With reference to any one of the second aspect, or the first to the second possible implementation manners of the second aspect, in a third possible implementation manner, the intermediate mixture includes any one of the following materials: air or resin.

15 **[0023]** With reference to any one of the second aspect, or the first to the third possible implementation manners of the second aspect, in a fourth possible implementation manner, the generating a first alloy layer includes: generating a first adhesive layer and a first co-sintered layer, thermally coupling the first adhesive layer to the circuit device, coupling the first co-sintered layer to the nanometal particle layer, and forming a sintered continuous phase structure at a contact portion between the first co-sintered layer and the nanometal particle layer.

20 **[0024]** With reference to any one of the second aspect, or the first to the fourth possible implementation manners of the second aspect, in a fifth possible implementation manner, the generating a second alloy layer includes: generating a second adhesive layer and a second co-sintered layer, thermally coupling the second adhesive layer to the heat sink fin, thermally coupling the second co-sintered layer to the nanometal particle layer, and forming a sintered continuous phase structure at a contact portion between the second co-sintered layer and the nanometal particle layer.

BRIEF DESCRIPTION OF DRAWINGS

25 **[0025]** To describe the technical solutions in the embodiments of the present invention or in the prior art more clearly, the following briefly describes the accompanying drawings required for describing the embodiments or the prior art. Apparently, the accompanying drawings in the following description show merely some embodiments of the present invention, and a person of ordinary skill in the art may still derive other drawings from these accompanying drawings without creative efforts.

30 **[0026]** FIG. 1A is a schematic sectional view of a packaging structure that includes an apparatus in the prior art;

[0027] FIG. 1 is a schematic sectional view of a packaging structure that includes an apparatus

according to a first embodiment of the present invention;

[0028] FIG. 2 is a schematic sectional view of a first embodiment of a thermal interface material layer in FIG. 1;

[0029] FIG. 3 is a schematic sectional view of a first embodiment of a first alloy layer in FIG. 2;

5 **[0030]** FIG. 4 is a schematic sectional view of a second embodiment of the first alloy layer in FIG. 2;

[0031] FIG. 5 is a schematic sectional view of a first embodiment of a second alloy layer in FIG. 2;

[0032] FIG. 6 is a schematic sectional view of a second embodiment of the second alloy layer in
10 FIG. 2; and

[0033] FIG. 7 is a flowchart of a method for manufacturing an apparatus according to a second embodiment of the present invention.

DESCRIPTION OF EMBODIMENTS

[0034] The following clearly and completely describes the technical solutions in the
15 embodiments of the present invention with reference to the accompanying drawings in the embodiments of the present invention. Apparently, the described embodiments are merely some but not all of the embodiments of the present invention. All other embodiments obtained by a person of ordinary skill in the art based on the embodiments of the present invention without creative efforts shall fall within the protection scope of the present invention.

20 **[0035]** FIG. 1 is a schematic sectional view of a packaging structure 100 that includes an apparatus according to a first embodiment of the present invention. A flip chip ball grid array packaging structure includes a solder ball 108, a substrate 107, an adhesive 106, a metal bump (BUMP) 102, a circuit device (for example, an integrated circuit die) 103, a thermal interface material layer 104, and a heat sink fin 105. The integrated circuit die 103 is coupled to the substrate
25 107 by using the metal bump 102. The metal bump 102 is protected by a bottom filler 101. The heat sink fin 105 is fastened on the substrate 107 by using the adhesive 106. The thermal interface material layer 104 is thermally coupled to the integrated circuit die 103 and the heat sink fin 105. In this specification, thermal coupling includes scenarios in which there is heat conduction between different layers, structures, or apparatuses. More specifically, the thermal interface material layer
30 104 may be located between the integrated circuit die 103 and the heat sink fin 105. A substrate of the integrated circuit die 103 is thermally coupled to the thermal interface material layer 104. Heat of the integrated circuit die 103 reaches the heat sink fin 105 by using the thermal interface material layer 104.

[0036] The integrated circuit die 103, the thermal interface material layer 104, and the heat sink fin 105 may be used as a part or all components of an apparatus, and the apparatus may be applied to, but is not limited to, the flip chip ball grid array packaging structure shown in the figure.

[0037] FIG. 2 is a schematic sectional view of a first embodiment of the thermal interface material layer 104 in FIG. 1. The thermal interface material layer 104 is thermally coupled to the die 103 and the heat sink fin 105, and includes a first alloy layer 109, a nanometal particle layer 110, and a second alloy layer 112.

[0038] The first alloy layer 109 is thermally coupled to the integrated circuit die 103 and the nanometal particle layer 110. More specifically, as shown in the figure, the first alloy layer 109 may be located on the integrated circuit die 103, and under the nanometal particle layer 110. That is, the first alloy layer 109 may be located between the integrated circuit die 103 and the nanometal particle layer 110. The first alloy layer 109 increases adhesive strength between the integrated circuit die 103 and the nanometal particle layer 110.

[0039] The nanometal particle layer 110 includes nanometal particles and an intermediate mixture. The intermediate mixture includes, but is not limited to, any one of the following materials: air or resin. The intermediate mixture is filled between multiple nanometal particles, and is used to enable the multiple nanometal particles to become a whole. The nanometal particles include, but are not limited to, silver. Diameters of the nanometal particles are not greater than 1 micrometer. In an embodiment, the diameters of the nanometal particles are between 50 nanometers and 200 nanometers. The nanometal particle layer 110 has a relatively low thermal resistance, and forms a relatively desirable heat conduction path.

[0040] The second alloy layer 112 is thermally coupled to the nanometal particle layer 110 and the heat sink fin 105. More specifically, as shown in the figure, the second alloy layer 112 may be located on the nanometal particle layer 110, and under the heat sink fin 105. That is, the second alloy layer 112 may be located between the nanometal particle layer 110 and the heat sink fin 105. The second alloy layer 112 increases adhesive strength between the nanometal particle layer 110 and the heat sink fin 105.

[0041] In an embodiment, a sintered continuous phase structure is formed at a contact portion between the first alloy layer 109 and the nanometal particle layer 110, sintered continuous phase structures are formed at contact portions between the nanometal particles, and a sintered continuous phase structure is formed at a contact portion between the second alloy layer 112 and the nanometal particle layer 110. The sintered continuous phase structure in this specification includes, but is not limited to, a whole structure formed by metal particles when metal atoms near contact portions of metal particles spread to metal particle interfaces and fuse with the metal particle interfaces because

the metal particles are sintered.

[0042] FIG. 3 is a schematic sectional view of a first embodiment of the first alloy layer 109 in FIG. 2. As shown in the figure, the first alloy layer 109 includes a first adhesive layer 114 and a first co-sintered layer 115. A co-sintered layer in this specification includes, but is not limited to, a metal layer that is generated in a packaging process and that fuses with a thermal interface material layer, and the metal layer and particles in the thermal interface material layer are co-sintered to form a heat flux path. The first adhesive layer 114 is thermally coupled to the integrated circuit die 103. The first co-sintered layer 115 is thermally coupled to the nanometal particle layer 110. A sintered continuous phase structure is formed at a contact portion between the first co-sintered layer 115 and the nanometal particle layer 110. Specifically, the first adhesive layer 114 may be located on the integrated circuit die 103, and the first co-sintered layer 115 may be located on the first adhesive layer 114, and under the nanometal particle layer 110. The first adhesive layer 114 includes, but is not limited to, any one of the following materials: titanium, chromium, nickel, or nickel/vanadium. The first adhesive layer 114 increases adhesive strength between the integrated circuit die 103 and the first co-sintered layer 115. The first co-sintered layer 115 includes, but is not limited to, any one of the following materials: silver, gold, or copper.

[0043] FIG. 4 is a schematic sectional view of a second embodiment of the first alloy layer 109 in FIG. 2. Compared with FIG. 3, the first alloy layer 109 in FIG. 4 further includes a first buffer layer 116 located between the first adhesive layer 114 and the first co-sintered layer 115. The first buffer layer 116 includes, but is not limited to, any one of the following materials: aluminum, copper, or nickel. The first buffer layer 116 provides a stress buffering function in a deformation caused by heat processing, and reduces a risk of a crack that appears between the integrated circuit die 103 and the thermal interface material layer 114, or in the middle of the thermal interface material layer 114, thereby increasing reliability of the apparatus.

[0044] FIG. 5 is a schematic sectional view of a first embodiment of the second alloy layer 112 in FIG. 2. As shown in the figure, the second alloy layer 112 includes a second co-sintered layer 118 and a second adhesive layer 117. The second co-sintered layer 118 is thermally coupled to the nanometal particle layer 110. A sintered continuous phase structure is formed at a contact portion between the second co-sintered layer 118 and the nanometal particle layer 110. The second adhesive layer 117 is thermally coupled to the heat sink fin 105. Specifically, the second co-sintered layer 118 may be located on the nanometal particle layer 110, and the second adhesive layer 117 may be located on the second co-sintered layer 118, and under the heat sink fin 105. The second co-sintered layer 118 includes, but is not limited to, any one of the following materials: silver, gold, or copper. The second adhesive layer 117 includes, but is not limited to, any one of the following materials:

titanium, chromium, nickel, or nickel/vanadium. The second adhesive layer 117 increases adhesive strength between the second co-sintered layer 115 and the heat sink fin 105.

[0045] FIG. 6 is a schematic sectional view of a second embodiment of the second alloy layer 112 in FIG. 2. Compared with FIG. 5, the second alloy layer 112 in FIG. 6 further includes a second buffer layer 119 located between the second adhesive layer 117 and the second co-sintered layer 118. The second buffer layer 119 includes, but is not limited to, any one of the following materials: aluminum, copper, nickel, or nickel/vanadium. The second buffer layer 119 provides a buffering function in a deformation caused by heat processing, and reduces a risk of a crack that appears between the thermal interface material layer and the heat sink fin 105, or in the middle of the thermal interface material layer 114, thereby increasing reliability of the apparatus.

[0046] In conclusion, because the thermal interface material layer in this embodiment of the present invention no longer includes a polymer material having a relatively low heat conductivity in a silver adhesive material, but instead, includes nanometal particles, the thermal interface material in this embodiment of the present invention has a relatively high thermal conductivity, greatly improves heat conduction efficiency of an entire heat path, and can better satisfy a heat dissipation requirement of a chip having high power consumption.

[0047] FIG. 7 is a flowchart 700 of a method for manufacturing an apparatus according to a second embodiment of the present invention. As shown in the figure, in step 702: generate a first alloy layer. In step 704: generate a nanometal particle layer by using nanometal particles and an intermediate mixture. Diameters of the nanometal particles are not greater than 1 micrometer. For example, the diameters of the nanometal particles are between 50 nanometers and 200 nanometers. The intermediate mixture includes, but is not limited to, any one of the following materials: air or resin. In an embodiment, the nanometal particles include, but are not limited to, silver. In step 706: generate a second alloy layer. In step 708: thermally couple the first alloy layer to the nanometal particle layer and the circuit device. In step 710, thermally couple the second alloy layer to the nanometal particle layer and a heat sink fin.

[0048] In an embodiment, the method further includes: forming a sintered continuous phase structure at a contact portion between the first alloy layer and the nanometal particle layer, forming sintered continuous phase structures at contact portions between the nanometal particles, and forming a sintered continuous phase structure at a contact portion between the second alloy layer and the nanometal particle layer.

[0049] In an embodiment, the method may be applied to, but is not limited to, a flip chip ball grid array structure.

[0050] In an embodiment, the generating a first alloy layer includes: generating a first adhesive

layer and a first co-sintered layer, thermally coupling the first adhesive layer to the circuit device, coupling the first co-sintered layer to the nanometal particle layer, and forming a sintered continuous phase structure at a contact portion between the first co-sintered layer and the nanometal particle layer. The first adhesive layer includes, but is not limited to, any one of the following materials: titanium, chromium, nickel, or nickel/vanadium. The first co-sintered layer includes, but is not limited to, any one of the following materials: silver, gold, or copper. In another embodiment, the generating a first alloy layer further includes: generating a first buffer layer between the first adhesive layer and the first co-sintered layer. The first buffer layer includes, but is not limited to, any one of the following materials: aluminum, copper, nickel, or nickel/vanadium.

[0051] In an embodiment, the generating a second alloy layer includes: generating a second adhesive layer and a second co-sintered layer, thermally coupling the second adhesive layer to the heat sink fin, thermally coupling the second co-sintered layer to the nanometal particle layer, and forming a sintered continuous phase structure at a contact portion between the second co-sintered layer and the nanometal particle layer. The second adhesive layer includes, but is not limited to, any one of the following materials: titanium, chromium, nickel, or nickel/vanadium. The second co-sintered layer includes, but is not limited to, any one of the following materials: silver, gold, or copper. In another embodiment, the generating a second alloy layer further includes: generating a second buffer layer between the second adhesive layer and the second co-sintered layer. The second buffer layer includes, but is not limited to, any one of the following materials: aluminum, copper, nickel, or nickel/vanadium.

[0052] The circuit device may include an integrated circuit die. The thermally coupling the first alloy layer to the circuit device includes: thermally coupling the first alloy layer to a substrate of the integrated circuit die.

[0053] What is disclosed above is merely exemplary embodiments of the present invention, and certainly is not intended to limit the protection scope of the present invention. Therefore, equivalent variations made in accordance with the claims of the present invention shall fall within the scope of the present invention.

CLAIMS

1. An apparatus, comprising:

a circuit device;

a heat sink fin; and

5 a thermal interface material layer, thermally coupled to the circuit device and the heat sink fin, and comprises:

a first alloy layer, thermally coupled to the circuit device;

a nanometal particle layer, thermally coupled to the first alloy layer, wherein the nanometal particle layer comprises multiple nanometal particles that are coupled to each other and an
10 intermediate mixture, and the intermediate mixture is filled between the multiple nanometal particles; and

a second alloy layer, thermally coupled to the nanometal particle layer and the heat sink fin.

2. The apparatus according to claim 1, wherein a sintered continuous phase structure is formed at a contact portion between the first alloy layer and the nanometal particle layer, sintered
15 continuous phase structures are formed at contact portions between the multiple nanometal particles, and a sintered continuous phase structure is formed at a contact portion between the second alloy layer and the nanometal particle layer.

3. The apparatus according to claim 1 or 2, wherein the multiple nanometal particles comprise silver.

20 4. The apparatus according to any one of claims 1 to 3, wherein diameters of the multiple nanometal particles are between 50 nanometers and 200 nanometers.

5. The apparatus according to any one of claims 1 to 4, wherein the apparatus is applied to a flip chip ball grid array structure.

6. The apparatus according to any one of claims 1 to 5, wherein the first alloy layer comprises
25 a first adhesive layer and a first co-sintered layer, the first adhesive layer is thermally coupled to the circuit device, the first co-sintered layer is coupled to the nanometal particle layer, and a sintered continuous phase structure is formed at a contact portion between the first co-sintered layer and the nanometal particle layer.

7. The apparatus according to claim 6, wherein the first adhesive layer comprises any one of
30 the following materials: titanium, chromium, nickel, or a nickel-vanadium alloy, and the first co-sintered layer comprises any one of the following materials: silver, gold, or copper.

8. The apparatus according to claim 6 or 7, wherein the first alloy layer further comprises a first buffer layer, located between the first adhesive layer and the first co-sintered layer, and the first buffer layer comprises any one of the following materials: aluminum, copper, nickel, or a

nickel-vanadium alloy.

9. The apparatus according to any one of claims 1 to 8, wherein the second alloy layer comprises a second adhesive layer and a second co-sintered layer, the second adhesive layer is thermally coupled to the heat sink fin, the second co-sintered layer is thermally coupled to the nanometal particle layer, and a sintered continuous phase structure is formed at a contact portion between the second co-sintered layer and the nanometal particle layer.

10. The apparatus according to claim 9, wherein the second adhesive layer comprises any one of the following materials: titanium, chromium, nickel, or a nickel-vanadium alloy, and the second co-sintered layer comprises any one of the following materials: silver, gold, or copper.

11. The apparatus according to claim 9 or 10, wherein the second alloy layer further comprises a second buffer layer, located between the second adhesive layer and the second co-sintered layer, and the second buffer layer comprises any one of the following materials: aluminum, copper, nickel, or a nickel-vanadium alloy.

12. The apparatus according to any one of claims 1 to 11, wherein the intermediate mixture comprises any one of the following materials: air or resin.

13. The apparatus according to any one of claims 1 to 12, wherein the circuit device comprises an integrated circuit die, and a substrate of the integrated circuit die is thermally coupled to thermal interface material layer.

14. A method for manufacturing an apparatus, comprising:

generating a first alloy layer;

generating a nanometal particle layer by using multiple nanometal particles that are coupled to each other and an intermediate mixture, and filling the intermediate mixture between the multiple nanometal particles; and

generating a second alloy layer,

thermally coupling the first alloy layer to the circuit device, thermally coupling the nanometal particle layer to the first alloy layer, and thermally coupling the second alloy layer to the nanometal particle layer and the heat sink fin.

15. The method according to claim 14, wherein the method further comprises: forming a sintered continuous phase structure at a contact portion between the first alloy layer and the nanometal particle layer, forming sintered continuous phase structures at contact portions between the multiple nanometal particles, and forming a sintered continuous phase structure at a contact portion between the second alloy layer and the nanometal particle layer.

16. The method according to claim 14 or 15, wherein diameters of the multiple nanometal particles are not greater than 1 micrometer.

17. The method according to any one of claims 14 to 16, wherein the intermediate mixture comprises any one of the following materials: air or resin.

18. The method according to any one of claims 14 to 17, wherein the generating a first alloy layer comprises: generating a first adhesive layer and a first co-sintered layer, thermally coupling
5 the first adhesive layer to the circuit device, coupling the first co-sintered layer to the nanometal particle layer, and forming a sintered continuous phase structure at a contact portion between the first co-sintered layer and the nanometal particle layer.

19. The method according to any one of claims 14 to 18, wherein the generating a second alloy layer comprises: generating a second adhesive layer and a second co-sintered layer, thermally
10 coupling the second adhesive layer to the heat sink fin, thermally coupling the second co-sintered layer to the nanometal particle layer, and forming a sintered continuous phase structure at a contact portion between the second co-sintered layer and the nanometal particle layer.