(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 November 2012 (29.11.2012)

WIPO | PCT

(10) International Publication Number
WO 2012/160063 A1

(51) International Patent Classification:
*H01L 21/768* (2006.01) *H01L 23/48* (2006.01)
*H01L 21/288* (2006.01)

(21) International Application Number:
PCT/EP2012/059503

(22) International Filing Date:
22 May 2012 (22.05.2012)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11305632.9 23 May 2011 (23.05.2011) EP
61/489,015 23 May 2011 (23.05.2011) US

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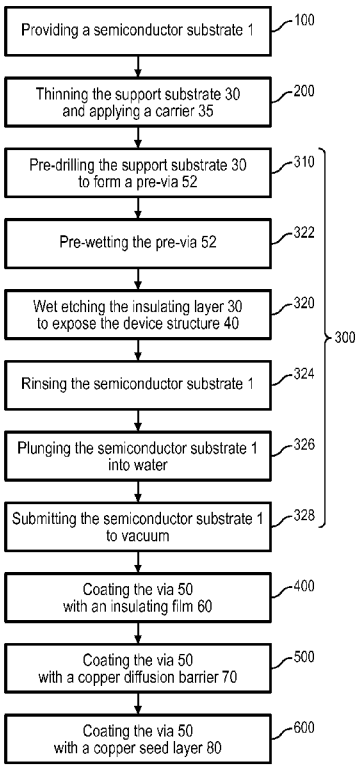
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK,

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(54) Title: METHOD FOR FORMING A VERTICAL ELECTRICAL CONNECTION IN A LAYERED SEMICONDUCTOR STRUCTURE

FIG. 7




(57) Abstract: The invention proposes a method for forming a vertical electrical connection (50) in a layered semiconductor structure (1), comprising the following steps: - providing (100) a layered semiconductor structure (1), said layered semiconductor structure (1) comprising: - a support substrate (20) including an first surface (22) and a second surface (24), - an insulating layer (30) overlying the first surface (22) of the support substrate (20), and - at least one device structure (40) formed in the insulating layer (30); and - drilling (300) a via (50) from the second surface of the support substrate (20) up to the device structure (40), in order to expose the device structure (40); characterized in that drilling (300) of the insulating layer is at least performed by wet etching (320).

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EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

**Declarations under Rule 4.17**:

— *of inventorship (Rule 4.17(iv))*

**Published**:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*