

The present invention relates to a method of setting up a conference call in a digital telephone switching system, in which the non-linearly-coded speech samples are converted into linearly-coded speech samples, which are added and then reconverted into non-linearly-coded speech samples, and to a circuit arrangement for carrying out such a method.

Already known from FR - A - 2 332 663 is a circuit arrangement for setting up a conference circuit in a digital exchange in which non-linearly-coded speech samples are converted into linearly-coded speech samples, added together and then converted back into non-linear speech samples. For this purpose an attenuation unit is connected between an input register and an output register on the one side and a processing unit on the other side. The attenuation unit contains a speech recognition unit which, depending on an amplitude threshold preset for a period, emits appropriate logic signals when the samples are below or above the threshold. As a result, speech samples of the speaking conference participant or participants which are above the threshold are passed on unattenuated and those which are below the threshold are passed on with a preset attenuation.

Also known is a digital conference circuit for a delta-modulated telephone exchange (US - A - 3,397,898) which contains a conference bridge which contains, for each conference participant, a data memory designed as a three-stage shift register and a detector. Each detector examines the speech samples input into the shift register for three successive bits of the same value which characterize the speech activity of a

conference participant. If three identical bits are recognized, an allocated counter is raised by one. A recognition circuit which follows compares the counter readings, recognizes the speaker assigned to the highest counter reading as active and resets all the counters to zero.

As the speech signals of the subscribers in digital telephone switching systems, particularly in PCM systems, are encoded into digital values in accordance with a non-linear - approximately logarithmic - characteristic and, at the receiving end, decoded into analog speech signals in accordance with a corresponding characteristic in order to improve the transmission quality, a conference call, i.e., a connection between more than two subscribers, cannot be set up by simply adding the digitized speech samples of the subscribers (DE-AS 18 03 222).

In a prior art method of this kind (DE-AS 24 45 094) the speech samples, after being encoded into PCM words consisting of, for instance, 8 bits in accordance with a non-linear characteristic, are converted into PCM words consisting of, for instance, 16 bits in a non-linear-to-linear code converter. As a vacant range remains between the positive and the negative range of the speech samples, the permissible amplitude range may be exceeded when subtotals are formed during the addition, during a conference call, of several speech samples having relatively large, unidirectional amplitudes. Distortions of the speech signals can, however, be avoided only if the total of the speech samples of all participants does not exceed the permissible amplitude range, i.e., does not lie within the vacant residual range of the permissible extended range for the subtotals. If the total of the

speech samples, too, does lie within the vacant residual range, the permissible amplitude range has been exceeded and the speech sample will be limited to the maximum permissible positive or negative value during the subsequent linear-to-non-linear code conversion. This results in a distortion of the analog speech signal to be restored prior to delivery to the receiver.

The object of the invention is to provide a method of and a circuit arrangement for setting up conference calls which reduces the distortion of the speech signals to a minimum.

According to the method, this object is achieved by the characteristics of Patent Claim 1 and the circuit arrangement is attained by the characteristics of Patent Claim 5. Special forms of the method are defined in Claims 2 to 4 and special forms of the circuit arrangement are defined in Claims 6 to 9.

The principal advantage of the invention is that an improvement in signal-to-noise performance is achieved. In addition, the round-trip loss required in a four-wire circuit with speech-signal amplification is maintained without increasing the insertion loss. Stability and echo conditions, determined by the hybrids terminating the four-wire circuits, are improved, and the distortion factor is reduced.

An embodiment of the invention will now be explained with reference to the accompanying drawing, in which:

Fig. 1 is a block diagram of a circuit arrangement according to the invention, and

Fig. 2 is a schematic of a sequence controller for the circuit arrangement of Fig. 1.

The conference circuit shown in Fig. 1 is connected to the switching network of a PCM exchange via a connection unit (not shown). Via a receiving line RX, a serial bit stream is transferred from the switching network to the conference circuit. From the conference circuit the outgoing serial bit stream is transferred back to the switching network via a transmitting line TX.

As is usual in PCM time-division-multiplex switching systems, the incoming bit stream is divided into 32 channels or time slots per frame, and each frame contains 256 bits. Each speech sample, i.e., each sample value of the speech signal, is encoded into a PCM word consisting of 8 bits, resulting in 256 quantizing steps. The sampling frequency is 8 kHz. 30 of the 32 channels are message channels, while channel No. 0 serves for frame synchronization and channel No. 16 is available for signalling information. In one embodiment, a circuit arrangement according to the invention is capable of forming 6 independent conference groups each consisting of up to 5 participants.

Each participant receives the sums of the speech samples of the other participants, the PCM speech samples being added in linearly coded form. If  $n$  persons participate in a conference, the conference circuit performs  $n$  different additions of  $n-1$  speech samples.

The speech samples are evaluated by taking the time integral thereof in a manner to be described later, and the speech samples of the participant found to be the loudest are added unattenuated, while the speech levels of all other participants are added after being attenuated by 12 dB.

The serial bit stream arriving via the receiving line RX is fed to a serial-to-parallel converter SPC and is passed from there, in the form of groups of 8 parallel bits, to a suppression circuit SIC. The two protocol bits representing the bit format of each channel are transferred from the converter SPC to the suppression circuit SIC - which detects idle channels by checking the bit formats and suppresses such channels for the further processing operations - via a line PB.

From the suppression circuit SIC the 8-bit words - each representing one speech sample - are fed, on the one hand, into a speech-sample buffer SSM, in which they are temporarily stored and, on the other hand, into an evaluation circuit EVC. In a first speech-sample comparator CFS, all speech samples of a conference are compared in groups. Each channel and, consequently, each participant is assigned a counter CNT (only one shown in the drawing). After every comparison of the speech samples of a conference group, the counter assigned to the loudest participant is increased by one count, while the counters assigned to the other participants are decreased by one count. The counters CNT count from 0 to 63. It thus takes 32 frames - i.e.,  $8 \times 125 \mu s = 4 \text{ ms}$  - at the most until a counter assigned to the loudest-talking participant has overtaken the counter assigned to another participant who was the loudest talker before. In this borderline case, a participant must thus deliver the speech samples with the highest intensity during 32 frames.

To determine the participant whose speech samples have the highest intensity, i.e., the loudest participant, the counts of the counters assigned to the participants

are compared in groups in a second comparator CFC. On the basis of this comparison the comparator CFC provides control bits, so-called attenuation bits, to a loss controller LFL, where they are temporarily stored. From there, the attenuation bits are transferred to a first code converter CCL, which performs a dual function. Firstly, it converts the non-linearly coded speech samples - produced by encoding the analog speech signal by a technique commonly referred to as "compressed coding" - into linearly coded speech samples such as are necessary for distortion-free addition. Each non-linearly coded PCM word is 8 bits long, as mentioned above, while the linearly coded speech samples each consist of 13 bits. This is indicated in Fig. 1 by the number of pairs of wires which compose the lines interconnecting the various subcircuits. From the speech-sample buffer SSM, the compressed speech samples are transferred to the first code converter CCL via a line consisting of 8 pairs of wires, while they leave this code converter as linearly coded speech samples via 13 pairs of wires. The attenuation bit is fed to the code converter CCL via one pair of wires.

Secondly, the code converter CCL attenuates all speech samples except that of the loudest participant. In one embodiment, an attenuation of 12 dB was chosen, but it is also readily possible to insert other attenuations. The code converter CCL is a PROM module, so that it is easy to set a different attenuation value. Which speech samples are attenuated and which are not attenuated is determined by the attenuation bit, which is set in the loss controller LFL.

The summation of the results of the speech-sample comparisons performed in the first comparator CFS, which is carried out in the counters CNT assigned to the individual participants, and the design of these counters produce a first time integration of the speech samples to be evaluated. To prevent any too frequent change of attenuation in response to instantaneous values, the counts are compared in the second comparator CFC not in each frame but only in every fourth frame. This produces a second time integration of the speech samples.

From the first code converter CCL, the successive speech samples of the participants and the associated attenuation bits are transferred to an adder ADD, in which they are summated to produce the summation signal. After every single addition they are temporarily stored in an accumulator ACC.

Following the addition, the speech samples are transferred to a second code converter LCC, in which they are converted back into linearly coded speech samples, which are transferred to a parallel-to-serial converter PSC via eight pairs of wires. From the converter PSC, the PCM words leave the conference circuit according to the invention in serial form via the line TX; they are transferred via the associated connection unit to the switching network and from there to the participants.

Between the PCM channels arriving in the conference circuit and the outgoing channels, a time displacement of 6 channels, i.e., of about 24  $\mu$ s, is obtained.

The conference circuit accordance to the invention also makes it possible to cut in on busy lines. In a private

branch exchange, for example, the calling party can cut in on the busy line of the called party, or an operator may intrude into an existing connection to announce a call from the public network.

Via the protocol bits, which, as mentioned above, are evaluated in the suppression circuit SIC, further information can be transferred and evaluated. An example is the information that a subscriber line is very long, which is known in the exchange; this information is used in order to subject the speech samples of the participant concerned to a smaller amount of attenuation.

Fig. 2 shows a sequence controller ROC, which receives the 4-MHz and 8-kHz signals and frame synchronisation signals FSYNC and provides control signals CS, which are applied to the individual subcircuits of the conference circuit according to the invention in order to control the time sequence of the operations performed there. The individual control lines running from the sequence controller ROC to the various subcircuits are not shown in order to simplify the illustration.

As all speech samples but one are attenuated in the conference circuit according to the invention before being summated, the probability that, and the amount by which, the amplitude of the speech-sum signal is exceeded are substantially reduced.

### Claims

1. Method of setting up a conference circuit in a digital telephone exchange, in which the non-linearly-coded speech samples are converted into linearly-coded speech samples, added together and then converted back into non-linearly coded speech samples, characterized in that the speech samples from the different participants in the conference circuit are chronologically integrated, the individual speech samples being compared with each other in a first comparator (CFS) and, on the basis of the result of the comparison, a counter (CNT) assigned to the loudest participant being raised by one and that counters (CNT) assigned to the other participants are lowered by one, that in a second comparator (CFC) connected thereafter the counter readings of the individual speech samples are compared with each other and an output signal characterizing the loudest participant is produced, and that the speech sample showing the highest intensity is passed to the addition unattenuated and the remaining speech samples are passed to the addition attenuated by a presettable value independent of the number of participants.



2. A method as claimed in Claim 1, characterized in that the speech samples are in each case compared with each other only after a preset number of time division multiplex frames.

3. A method as claimed in either one of Claims 1 or 2, characterized in that, in each case, the switching over from the unattenuated transmission of the speech samples of one participant to the unattenuated transmission of the speech samples of another participant takes place only after a preset number of time division multiplex frames.

4. A method as claimed in any one of the preceding Claims, characterized in that the preset attenuation value is 12 dB.

5. A circuit arrangement for implementation of the method as claimed in Claim 1, which, for the purpose of setting up a conference circuit in a digital telecommunication system, includes a first code converter (CCL) by which the individual non-linearly-coded speech samples from the participants are converted into linearly-coded values, with a summing adding circuit (ADD) which adds the converted values together, and also with a second code converter (LLC) which converts the sum values into non-linearly-coded speech samples,



characterized in that the circuit arrangement contains an evaluation circuit (EVC) which comprises a first comparator (CFS) which compares the incoming speech samples and a counter (CNT) for each of the participants and also a second comparator (CFC) connected behind the counters (CNT), so that the incoming speech samples are evaluated during an integration period in such a way that the conference participant with the highest speech signal intensity is ascertained, and that that participant's speech samples are passed to the adding circuit unattenuated and that the speech samples of the other participants are passed to the adding circuit attenuated by a presetable value independent of the number of participants.

6. A circuit arrangement as claimed in Claim 5, characterized in that the counters (CNT) are so dimensioned that, after a change of the active speaker, a participant is ascertained as being the loudest after not more than 4ms.

7. A circuit arrangement as claimed in Claim 5 or 6, characterized in that the output signal of the second comparator (CFS) is passed to an attenuation control (LFL) which emits a control signal to the first code converter (CCL), on the basis of which signal the speech sample converted there in each case is attenuated or not attenuated.



8. A circuit arrangement as claimed in any one of Claims 5 to 7, characterized in that the second comparator (CFC) in each case compares the counter readings after four time division multiplex frames.

9. A circuit arrangement as claimed in any one of Claims 5 to 8, characterized in that it is provided with a suppression circuit (SIC) which, on the basis of a checking of bit formats, recognises and suppresses unoccupied channels.



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