This Sheet Has Been Replaced

A B S T R A C T

A DRAM having on-chip ECC (30) and both bit and word redundancy that have been optimized to support the on-chip ECC. The bit line redundancy features a switching network that provides an any-for-any substitution for the bit lines in the associated memory array. The word line redundancy is provided in a separate array section (20), and has been optimized to maximize signal while reducing soft errors. The array stores data in the form of error correction words (ECWs) on each word line. A first set of data lines (formed in a zig-zag pattern to minimize unequal capacitive loading on the underlying bit lines) are coupled to read out an ECW as well as the redundant bit lines. A second set of data lines receive the ECW as corrected by bit line redundancy, and a third set of data lines receive the ECW as corrected by the word line redundancy. The third set of data lines are coupled to the ECC block, which corrects errors encountered in the ECW. The ECC circuitry (30) is optimized to reduce the access delays introduced by carrying out on-chip error correction. The ECC block (30) provides both the corrected data bits and the check bits to an SRAM (40). Thus, the check bits can be externally accessed, improving testability of the memory chip. At the same time, having a set of interrelated bits in the SRAM (40) improves access performance when using multi-bit access modes, which compensates for whatever access delays are introduced by the ECC. To maximize the efficiency of switching from mode to mode, the modes are set as a function of received address signals.