ABSTRACT

PROGRAMMABLE MULTI-PROCESSOR INTERRUPT CONTROLLER SYSTEM WITH A PROCESSOR INTEGRATED LOCAL INTERRUPT CONTROLLER

A multi-processor programmable interrupt controller system that includes: an I/O interrupt controller for receiving interrupt requests from an I/O subsystem; multiple processor interrupt controllers, each associated with a specific processor for dispensing of accepted interrupts; and an interrupt controller bus primarily for the transmission of interrupt requests between interrupt controller units and for bus and priority arbitration, using a standard message format and arbitration protocol. The system is implemented, in part, by incorporating the processor interrupt controller with its associated processor into a single integrated circuit. The common system bus which normally carries all system traffic is not used for interrupt request messages. The interrupt controller bus is used for this purpose and thus results in a more efficient system by relieving the system bus of interrupt service requests and the related interrupt request traffic.

This Sheet Has Been Replaced

