DESCRIPTION

METHOD FOR DESIGNING SOI WAFER AND METHOD FOR MANUFACTURING SOI WAFER

TECHNICAL FIELD

[0001]

The present invention relates to a method for designing and manufacturing an SOI wafer having an SOI layer formed on a buried insulator layer, and more particularly to a method for designing and manufacturing an SOI wafer suitable for photolithography that is to be performed after manufacturing.

BACKGROUND ART

[0002]

In recent years, SOI wafers have been used in device fabrication as semiconductor substrates having a multilayer film structure. For example, various devices, such as CPUs, logics, memories, physical sensors related to MEMS (Micro-Electro-Mechanical-Systems), biosensors, and RF devices, are fabricated by using SOI wafers.

[0003]

As methods for fabricating the SOI wafers, wafer bonding methods and a SIMOX method are generally known. An ion implantation delamination method (also referred to as the SMART-CUT (a registered trademark) method), which is one of the wafer bonding methods, is proposed in Patent Document 1. In this method, an oxide film is formed on at least one of two silicon wafers, at least one of hydrogen ions and rare gas ions are implanted into a main surface of one of the wafers (a bond wafer) to form an ion-implanted layer in the interior of the

wafer. The ion-implanted surface is then brought into close contact with a main surface of the other silicon wafer through the oxide film and the resultant wafer is then delaminated at the ion-implanted layer by performing a heat treatment at a temperature in the range of 300°C to 600°C, or more than that. The ion implantation delamination method has an advantage in that an SOI wafer having a thin SOI layer with a film thickness uniformity of ±10 nm or less can be readily fabricated and an advantage in that the delaminated bond wafer can be reused several times to reduce cost.

[0004]

On the other hand, in the SIMOX method, high concentration oxygen ions are implanted into the interior of a silicon wafer to form an oxygen ion-implanted layer, a buried oxide film (a BOX layer) is then formed in the silicon wafer by performing an annealing process at a high temperature of approximately 1300°C, and a layer of its surface side is used as the SOI layer.

[0005]

A device pattern is then formed on the SOI wafer fabricated in the above manner. In this case, the feature size of pattern exhibits a wide range of pattern sizes from a relatively large size pattern for used in MEMS, RF devices and the like to a fine pattern for used in the latest CPUs, logics, memories and the like that have been significantly shrunken. Photolithography, which is one of the most important processes used for pattern formation in manufacture of various devices, has been used to form device patterns of various design rules.

[0006]

In accordance with the feature size and so on, a wavelength from a visible light region to a deep ultraviolet light (DUV) region is used as the wavelength of an exposure light utilized for a photolithography operation. More specifically, the exposure light wavelength used herein is changed according to the design rules and so on. For example, in the case of formation of a relatively large size pattern such as the above mentioned MEMS, a mercury lamp having a wavelength of 436 nm or 365 nm is used. An excimer laser having a wavelength of 248 nm or 193 nm is used for the latest CPUs, logics, and memories, for exmaple. It can be thought that an extreme ultraviolet light (EUV) having a wavelength of 13.5 nm will be used as the exposure light in future.

[0007]

For the purpose of improving line width uniformity of an image of the pattern exposed to a light on the wafer, Patent Document 2 discloses an exposing device that is provided with a digital micro device as a reflection element array including a plurality of mirror elements that are each operable to control the reflection direction of an illumination light and controlling illumination distribution by adjusting reflection angles of the mirror elements separately from each other. Patent Document 2 also discloses use of an exposure light wavelength of 248 nm or 193 nm and use of the SOI wafer as a wafer subjected to photolithography.

CITATION LIST

PATENT LITERATURE

[0008]

Patent Document 1:Japanese Unexamined Patent publication

(Kokai) No.H05-211128

Patent Document 2:Pamphlet of International Publication No.WO2006/085626

SUMMARY OF INVENTION

[0009]

In the above-described photolithography operation in a device manufacturing process, there has been a problem in that the reflection rate of the exposure light varies widely due to variation in the SOI layer thickness in a plane of the SOI wafer and the intensity of exposure to a resist thereby varies so that unevenness of exposure is created. As a result, pattern blurring and pattern shift are created in a developed pattern, thereby resulting in a difference in the developed pattern from the corresponding designed pattern. A difference from design may also be created in pattern formation of the SOI wafer, which is performed by subsequent steps such as etching, film formation, and ion implantation, thereby resulting in variation in device electric characteristics.

[0010]

The present invention was accomplished in view of the above-described problems, and its object is to provide a method for designing an SOI wafer and a method for manufacturing an SOI wafer that enable the variation in the reflection rate of the exposure light due to the variation in the SOI layer thickness of the SOI wafer and hence variation in the exposure state of a resist to be inhibited in a photolithography operation.

[0011]

To achieve this object, the present invention provides a method for designing an SOI wafer that has an SOI layer formed on a buried insulator layer and is

suitable for photolithography with an exposure light having a wavelength λ, the method comprising designing a thickness of the buried insulator layer of the SOI wafer on the basis of the wavelength λ of the exposure light.

[0012]

When the thickness of the buried insulator layer of the SOI wafer is designed on the basis of the wavelength λ of the exposure light as above, an SOI wafer can be designed which enables inhibition of the variation in the reflection rate of the exposure light due to the variation in the SOI layer thickness and hence inhibition of the variation in the exposure state of the resist when the photolithography operation is performed on the SOI wafer and enables pattern formation with high precision.

[0013]

In this method, the thickness of the buried insulator layer of the SOI wafer can be designed as a thickness d satisfying an expression $d=(1/2)\times(\lambda/n)\times A$, wherein d represents the thickness of the buried insulator layer, n represents a refractive index of the buried insulator layer, and A represents an arbitrary positive integer.

When the thickness of the buried insulator layer of the SOI wafer is designed as a thickness d satisfying an expression $d=(1/2)\times(\lambda/n)\times A$, wherein d represents the thickness of the buried insulator layer, n represents a refractive index of the buried insulator layer, and A represents an arbitrary positive integer as above, the thickness of the buried insulator layer of the SOI wafer can be concretely designed on the basis of the wavelength λ of the exposure light utilized for the photolithography operation, and the SOI wafer can be

designed which enables inhibition of the variation in the reflection rate of the exposure light due to the variation in the SOI layer thickness and hence inhibition of the variation in the exposure state of the resist when the photolithography operation is performed on the SOI wafer.

[0014]

In the method, the buried insulator layer can be any one of a silicon oxide film, a silicon nitride film, and a silicon oxynitride film, or a laminated insulator layer formed as a multilayer thereof.

Even when various insulator films, such as any one of a silicon oxide film, a silicon nitride film, and a silicon oxynitride film, or a laminated insulator layer formed as a multilayer thereof, are used as the buried insulator layer, the SOI wafer can be designed which enables inhibition of the variation in the reflection rate of the exposure light due to the variation in the SOI layer thickness and hence inhibition of the variation in the exposure state of the resist in the photolithography operation in accordance with the present invention.

[0015]

Furthermore, the present invention provides a method for manufacturing an SOI wafer that has an SOI layer formed on a buried insulator layer and is suitable for photolithography with an exposure light having a wavelength λ, the method comprising the steps of: designing a thickness of the buried insulator layer of the SOI wafer on the basis of the wavelength λ of the exposure light utilized for the photolithography that is to be performed on the SOI wafer after manufacturing; and fabricating the SOI wafer that has the SOI layer

formed on the buried insulator layer having the designed thickness.

[0016]

With the manufacturing method including the steps of: designing a thickness of the buried insulator layer of the SOI wafer on the basis of the wavelength λ of the exposure light utilized for the photolithography that is to be performed on the SOI wafer after manufacturing; and fabricating the SOI wafer that has the SOI layer formed on the buried insulator layer having the designed thickness as above, the SOI wafer can be manufactured which enables inhibition of the variation in the reflection rate of the exposure light due to the variation in the SOI layer thickness and hence inhibition of the variation in the exposure state of the resist when the photolithography operation is performed on the SOI wafer and enables pattern formation with high precision.

[0017]

In the manufacturing method, the thickness of the buried insulator layer of the SOI wafer can be designed as a thickness d satisfying an expression $d=(1/2)\times(\lambda/n)\times A$, wherein d represents the thickness of the buried insulator layer, n represents a refractive index of the buried insulator layer, and A represents an arbitrary positive integer.

When the thickness of the buried insulator layer of the SOI wafer is designed as a thickness d satisfying an expression $d=(1/2)\times(\lambda/n)\times A$, wherein d represents the thickness of the buried insulator layer, n represents a refractive index of the buried insulator layer, and A represents an arbitrary positive integer as above, the thickness of the buried insulator layer of the SOI wafer

can be concretely designed on the basis of the wavelength λ of the exposure light utilized for the photolithography operation, and the SOI wafer can be manufactured which enables inhibition of the variation in the reflection rate of the exposure light due to the variation in the SOI layer thickness and hence inhibition of the variation in the exposure state of the resist when the photolithography operation is performed on the SOI wafer.

[0018]

In the manufacturing method, the buried insulator layer can be any one of a silicon oxide film, a silicon nitride film, and a silicon oxynitride film, or a laminated insulator layer formed as a multilayer thereof.

Even when various insulator films, such as any one of a silicon oxide film, a silicon nitride film, and a silicon oxynitride film, or a laminated insulator layer formed as a multilayer thereof, are used as the buried insulator layer, the SOI wafer can be manufactured which enables inhibition of the variation in the reflection rate of the exposure light due to the variation in the SOI layer thickness and hence inhibition of the variation in the exposure state of the resist in the photolithography operation in accordance with the present invention.

[0019]

In the inventive method for manufacturing an SOI wafer that has an SOI layer formed on a buried insulator layer and is suitable for photolithography with an exposure light having a wavelength λ, at least the steps of: designing the thickness of the buried insulator layer of the SOI wafer on the basis of the wavelength λ of the exposure light utilized for the photolithography

operation that is to be performed on the SOI wafer after manufacturing; and fabricating the SOI wafer that has the SOI layer formed on the buried insulator layer having the designed thickness are included. The method can therefore manufacture the SOI wafer which enables inhibition of the variation in the reflection rate of the exposure light due to the variation in the SOI layer thickness and hence inhibition of the variation in the exposure state of the resist when the photolithography operation is performed on the SOI wafer and enables pattern formation with high precision. In addition, the reflection rate of the light to which the SOI wafer manufactured by the present invention is exposed can be made to be equivalent to that in the case of a bulk silicon (a silicon single crystal). The present invention thus has also an advantage in that photolithography conditions (the thickness of the resist, the thickness of a film for preventing reflection, exposure conditions and so on) for the bulk silicon can be used without alteration.

BRIEF DESCRIPTION OF DRAWINGS

[0020]

FIG. 1 is a diagram showing the result of a simulation of a relation among the SOI layer thickness, the buried insulator layer thickness, and the reflection rate in the case of a wavelength of 193 nm;

FIG. 2 is a diagram showing the result of a simulation of a relation among the SOI layer thickness, the buried insulator layer thickness, and the reflection rate in the case of a wavelength of 248 nm;

FIG. 3 is a diagram showing the result of a simulation of a relation among the SOI layer thickness,

the buried insulator layer thickness, and the reflection rate in the case of a wavelength of 365 nm;

FIG. 4 is a diagram showing the result of a simulation of a relation among the SOI layer thickness, the buried insulator layer thickness, and the reflection rate in the case of a wavelength of 436 nm;

FIG. 5 is a diagram showing the result of measurement of the reflection rate with respect to the variation in the SOI layer thickness when being exposed to an ArF laser having a wavelength of 193 nm;

FIG. 6 is a diagram showing the results of Example 1 and Comparative Example 1;

FIG. 7 is a diagram showing the results of Example 2 and Comparative Example 2;

FIG. 8 is a diagram showing the results of Example 3 and Comparative Example 3;

FIG. 9 is a diagram showing the results of Example 4 and Comparative Example 4; and

FIG. 10 is a schematic view showing an example of an SOI wafer being designed and manufactured by the method for designing and manufacturing an SOI wafer of the present invention.

DESCRIPTION OF EMBODIMENTS

[0021]

Hereinafter, embodiments of the present invention will be described, but the present invention is not limited to these embodiments.

Conventionally, in the photolithography operation in a device fabrication process, there has been a problem in that the reflection rate of the exposure light varies widely due to the variation in the SOI layer thickness in a plane of the SOI wafer and the

intensity of exposure to the resist thereby varies so that unevenness of exposure is created. As a result, a difference in the developed resist pattern from the corresponding designed pattern may be created and a difference from design may also be created in pattern formation of the SOI wafer, which is performed by subsequent steps such as etching, film formation, and ion implantation, thereby resulting in variation in device electric characteristics.

[0022]

In view of this, the present inventor repeatedly and keenly conducted studies to solve the problem. The present inventor focused attention on the wavelength of the exposure light and the thickness of the buried insulator layer and simulated the relation between the SOI layer thickness and the reflection rate of the exposure light when the wavelength of the exposure light and the buried insulator layer thickness are changed.

[0023]

FIG. 1 shows the result of the simulation of the relation between the reflection rate of the exposure light and the SOI layer thickness when SOI wafers each having a different buried insulator layer thickness are exposed to an ArF laser having a wavelength λ of 193 nm. The variation in the reflection rate is represented by a shade of color in FIG. 1 and a color closer to white exhibits a higher reflection rate.

It can be seen from the relation among the buried insulator layer thickness, the SOI layer thickness, and the reflection rate in FIG. 1 that the reflection rate does not vary (the color exhibiting the reflection rate does not vary) with respect to the variation in the SOI layer thickness when the buried insulator layer

thickness is approximately 62 nm, 124 nm, and 186 nm.

[0024]

FIG. 5 shows the result of measurement of the reflection rate with respect to the variation in the SOI layer thickness when an SOI wafer having a buried insulator layer thickness of 145 nm is exposed to the ArF laser having a wavelength of 193 nm.

As shown in FIG. 5, when the SOI layer thickness is equal to or less than 30 nm, the reflection rate varies widely due to the variation in the SOI layer thickness. When the photolithography operation is performed with the ArF laser on an SOI wafer having a SOI layer thickness of 30 nm or less, the exposure state of a photoresist applied to the surface of the SOI wafer therefore varies according to a position in a plane of the SOI layer when there is thickness distribution in the plane of the SOI layer, and this causes the difference in the developed resist pattern after exposure from the designed pattern. As a result, the variation in characteristics of devices being fabricated is induced.

[0025]

The present inventor thought on the basis of these results that selecting a film thickness that is properly designed for the wavelength λ of the exposure light utilized for resist exposure in the photolithography operation as the thickness of the buried insulator layer of the SOI wafer enables the variation in the reflection rate to be avoided even though the SOI layer thickness varies. The present inventor further conducted simulations and experiments in various conditions and carefully examined them, thereby bringing the present invention to completion.

[0026]

FIG. 10 shows a schematic view of an example of the SOI wafer being designed and manufactured by the method for designing an SOI wafer and the method for manufacturing an SOI wafer of the present invention. As shown in FIG. 10, in the SOI wafer 10, the SOI layer 1 is formed on the buried insulator layer 2 on the base wafer 3, which is a supporting substrate.

A wavelength in the range from the visible light region to the DUV region is used as the wavelength of the exposure light utilized for the photolithography operation being performed on the SOI wafer 10. The wavelength is appropriately determined according to the feature size on the SOI wafer 10 and so on.

[0027]

In the method for designing an SOI wafer of the present invention, the thickness of the buried insulator layer of the SOI wafer is designed on the basis of the wavelength λ of the exposure light such that the variation in the reflection rate of the exposure light due to the variation in the SOI layer thickness is inhibited to design an SOI wafer suitable for the photolithography with the exposure light having the wavelength λ.

More specifically, the buried insulator layer thickness can be designed as a thickness d satisfying an expression $d=(1/2)\times(\lambda/n)\times A$, wherein d represents the thickness of the buried insulator layer, n represents the refractive index of the buried insulator layer, and A represents an arbitrary positive integer.

[0028]

Designing the thickness of the buried insulator layer of the SOI wafer in this manner realizes design of

the SOI wafer that enables inhibit of the variation in the reflection rate of the exposure light due to the variation in the SOI layer thickness and hence inhibit of the variation in the exposure state of the resist when the photolithography operation is performed on the SOI wafer and enables pattern formation with high precision.

[0029]

The results of the simulations of the relation between the SOI layer thickness and the reflection rate of the exposure light with respect to the buried insulator layer thickness when the SOI wafers were exposed to the exposure light having a wavelength λ are given in FIGS. 1 to 4 and Table 1. In the simulations conducted herein, silicon wafers were used as the base wafers, silicon oxide films were used as the buried insulator layers. The refractive indexes of the buried insulator layers were given in Table 1.

As described above, FIG. 1 shows the simulation result when the ArF laser having a wavelength λ of 193 nm was used. As shown in FIG. 1, the variation in the reflection rate with respect to the variation in the SOI layer thickness is substantially eliminated when the buried insulator layer thickness is approximately a positive multiple of 62 nm. Here, the positive multiple of 62 nm is equal to a value obtained by the expression $(1/2)\times(\lambda/n)\times A$.

[0030]

FIG. 2 shows the simulation result when a KrF laser having a wavelength λ of 248 nm was used. As shown in FIG. 2, the variation in the reflection rate with respect to the variation in the SOI layer thickness is substantially eliminated when the buried insulator

layer thickness is approximately a positive multiple of 82.2 nm.

FIG. 3 shows the simulation result when i-line of a mercury lamp having a wavelength λ of 365 nm was used. As shown in FIG. 3, the variation in the reflection rate with respect to the variation in the SOI layer thickness is substantially eliminated when the buried insulator layer thickness is approximately a positive multiple of 123.8 nm.

FIG. 4 shows the simulation result when g-line of a mercury lamp having a wavelength λ of 436 nm was used. As shown in FIG. 4, the variation in the reflection rate with respect to the variation in the SOI layer thickness is substantially eliminated when the buried insulator layer thickness is approximately a positive multiple of 148.6 nm.

When using EUV having a wavelength λ of 13.5 nm (not shown), the variation in the reflection rate with respect to the variation in the SOI layer thickness was substantially eliminated when the buried insulator layer thickness was approximately a positive multiple of 6.9 nm.

[0031]

Table 1 summarizes the above results. As shown in the results, designing the buried insulator layer thickness d so as to satisfy the expression $d=(1/2)\times(\lambda/n)\times A$ ensures a constant reflection rate of the exposure light without being affected by the variation in the SOI layer thickness, and the constant reflection rate can be made to be equivalent to a reflection rate in a state where the buried insulator layer thickness is zero, i.e., in a state where a bulk silicon is used.

[0032]

(Table 1)

	SIMULATION 1	SIMULATION 2	SIMULATION 3	SIMULATION 4	SIMULATION 5
WAVELENGTH λ OF EXPOSURE LIGHT (nm)	193	248	365	436	13.5
REFRACTIVE INDEX OF BURIED INSULATOR LAYER	1.5628	1.5086	1.4746	1.4667	0.9765
λ/2n	62	82.2	123.8	148.6	6.9

[0033]

In the method, the buried insulator layer can be any one of a silicon oxide film, a silicon nitride film, and a silicon oxynitride film, or a laminated insulator layer formed as a multilayer thereof.

When the buried insulator layer is the silicon nitride film or silicon oxynitride film as above, the buried insulator layer thickness may be designed by using the refractive index of the buried insulator layer as well as the silicon oxide film.

In the case of the laminated insulator layer formed of a plurality of buried insulator layers, the thicknesses of the buried insulator layers may be each designed such that the product (d×n) of the buried insulator layer thickness and its refractive index is calculated at each buried insulator layer in the laminated insulator layer and the sum of the products of all layers satisfies the expression $(1/2)\times\lambda\times A$. For example, when the laminated insulator layer has two layers, it may be designed so as to satisfy an expression $d1\times n1+d2\times n2=(1/2)\times\lambda\times A$, wherein d1 and n1 represent the thickness and refractive index of a first buried insulator layer respectively and d2 and n2 represent the thickness and refractive index of a second

buried insulator layer respectively.

[0034]

The present invention realizes design of a suitable SOI wafer for photolithography by which the variation in the reflection rate of the exposure light due to the variation in the SOI layer thickness can be inhibited in the photolithography operation and the variation in the exposure state of the resist can be thereby inhibited, even when various buried insulator layers are used as described above.

[0035]

Next, the method for manufacturing an SOI wafer of the present invention will be described.

First, the thickness of the buried insulator layer of the SOI wafer is designed on the basis of the wavelength λ of the exposure light utilized for photolithography that is to be performed on the SOI wafer after manufacturing such that the variation in the reflection rate of the exposure light due to the variation in the SOI layer thickness is inhibited, in the same manner as the above-described method for designing an SOI wafer of the present invention.

[0036]

More specifically, the buried insulator layer thickness can be designed as a thickness d satisfying the expression $d=(1/2)\times(\lambda/n)\times A$, wherein d represents the thickness of the buried insulator layer, n represents the refractive index of the buried insulator layer, and A represents an arbitrary positive integer.

Next, the SOI wafer 10 having the SOI layer 1 formed on the buried insulator layer 2 on the base wafer 3, which is a supporting substrate, is fabricated as shown in FIG. 10. In the fabrication, the thickness of

the buried insulator layer 2 is the designed thickness.

[0037]

The SOI wafer 10 can be fabricated, for example, by the bonding method in which two silicon single crystal wafers are prepared for the base wafer 3 and the bond wafer, the buried insulator layer 2 having the above designed thickness is formed on at least one of the wafers, the base wafer 3 is bonded to the bond wafer, and the bond wafer is thinned.

[0038]

The thinning step for forming the SOI layer 1 of the SOI wafer 10 can be performed by grinding and polishing, or the ion implantation delamination method. The ion implantation delamination method is a technique for obtaining an SOI wafer, for example, as follows: a silicon oxide film is formed on at least one of two silicon single crystal wafers; at least one of hydrogen ions and rare gas ions are implanted from the surface of one of the wafers (the bond wafer) to form a micro bubble layer (an enclosed layer) at the close vicinity of the surface in the interior of the wafer; the ion-implanted surface of the bond wafer is then brought into close contact with the other wafer (the base wafer) through the silicon oxide film; a heat treatment (a delamination heat treatment) is then performed to delaminate the bond wafer as a thin film such that the micro bubble layer becomes a cleavage plane (a delaminated plane); and a heat treatment (a bonding heat treatment) is further performed to firmly bond the two silicon single crystal wafers together. An SOI wafer having a thin SOI layer with very high thickness uniformity can be obtained with relative ease by the ion implantation delamination method.

The ion implantation delamination method enables easy and highly accurate control of the thickness of the SOI layer and the BOX layer and is particularly preferable to be used in the method for manufacturing an SOI wafer of the present invention.

[0039]

Various heat treatments may be then applied according to the SOI wafer being fabricated.

Manufacturing the SOI wafer in this manner realizes manufacture of the suitable SOI wafer for photolithography that enables inhibition of the variation in the reflection rate of the exposure light due to the variation in the SOI layer thickness and hence inhibition of the variation in the exposure state of the resist when the photolithography operation is performed on the SOI wafer and enables pattern formation with high precision. As a result, variation in device patterns formed by developing after exposure in the photolithography operation or by subsequent processes (e.g., etching, film formation, and ion implantation) can be substantially eliminated, thereby achieving device patterns as designed.

[0040]

Moreover, since the reflection rate can be made to be equivalent to a reflection rate in a state where a bulk silicon (or a bulk silicon on which a film identical to that formed on the SOI surface is formed) is used, photolithography conditions such as thickness design of a film used in the photolithography operation, e.g., a resist film, a film for preventing reflection, and a topcoat film (in the case of immersion photolithography) can be identical to those used for the bulk silicon, and this enables simplification of the

photolithography.

[0041]

In the method, the buried insulator layer can be any one of a silicon oxide film, a silicon nitride film, and a silicon oxynitride film, or a laminated insulator layer formed as a multilayer thereof.

When the buried insulator layer is the silicon nitride film or silicon oxynitride film, the buried insulator layer thickness may be designed by using the refractive index of the buried insulator layer as well as the silicon oxide film.

[0042]

As described above, in the case of the laminated insulator layer formed of a plurality of buried insulator layers, the thicknesses of the buried insulator layers may be each designed such that the product (d×n) of the buried insulator layer thickness and its refractive index is calculated at each buried insulator layer in the laminated insulator layer and the sum of the products of all layers satisfies the expression $(1/2)\times\lambda\times A$.

[0043]

The present invention realizes manufacture of the suitable SOI wafer for photolithography by which the variation in the reflection rate of the exposure light due to the variation in the SOI layer thickness can be inhibited in the photolithography operation and the variation in the exposure state of the resist can be thereby inhibited, even when various buried insulator layers are used as described above.

[0044]

In the embodiments described above, the silicon oxide film, the silicon nitride film, and the silicon

oxynitride film are exemplified as the buried insulator layer 2. In the present invention, however, insulator films made of high permittivity materials (high-k films) such as HfO_2, ZrO_2, La_2O_3, and TiO_2 can also be employed.

EXAMPLE

[0045]

The present invention will be more specifically described below with reference to Examples and Comparative Examples, but the present invention is not limited these examples.

[0046]

(Example 1)

An SOI wafer suitable for photolithography with an exposure light having a wavelength λ was manufactured by the method for designing an SOI wafer and the method for manufacturing an SOI wafer of the present invention. The reflection rate with respect to the variation in the SOI layer thickness was evaluated when the manufactured SOI wafer was exposed to the exposure light having the wavelength λ. In Example 1, the wavelength λ of the exposure light was 193 nm, and the buried insulator layer thickness designed on the basis of the wavelength λ was 124 nm (See Table 1).

[0047]

The evaluation result is given in FIG. 6. Referring to FIG. 6, it can be seen that the reflection rate with respect to the variation in the SOI layer thickness did not vary but stayed constant. On the other hand, it can be seen that, in the later-described Comparative Example 1, the reflection rate with respect to the variation in the SOI layer thickness varied widely.

It can be accordingly confirmed that the method for designing an SOI wafer and the method for manufacturing an SOI wafer of the present invention realize design and manufacture of the suitable SOI wafer for photolithography, and when the SOI wafer designed and manufactured by the invention is used in the photolithography operation, the variation in the reflection rate of the exposure light due to the variation in the SOI layer thickness can be inhibited and the variation in the exposure state of the resist can be thereby inhibited. The SOI wafer also enables pattern formation with high precision.

[0048]

(Examples 2 to 4)

The conditions of the wavelength λ of the exposure light and the buried insulator layer thickness designed on the basis of the wavelength λ in Example 1 were changed to evaluate the reflection rate in the same manner as in Example 1 (See Table 1). In Example 2, the wavelength λ was 248 nm and the buried insulator layer thickness was 164.5 nm. In Example 3, the wavelength λ was 365 nm and the buried insulator layer thickness was 123.8 nm. In Example 4, the wavelength λ was 436 nm and the buried insulator layer thickness was 148.6 nm.

[0049]

The evaluation results are given in FIGS. 7 to 9. Referring to FIGS. 7 to 9, in all of these examples, the reflection rate with respect to the variation in the SOI layer thickness did not vary but stayed constant. The results exhibited the same tendency as Example 1.

[0050]

(Comparative Examples 1 to 4)

An SOI wafer was manufactured in the same manner as Examples 1 to 4 except that the buried insulator layer thickness d was designed to be a thickness not satisfying the expression $d=(1/2)\times(\lambda/n)\times A$, and the reflection rate was evaluated in the same manner as Example 1. In Comparative Example 1, the buried insulator layer thickness was 145 nm. In Comparative Examples 2 to 4, the buried insulator layer thickness was 200 nm.

The results are given in FIGS. 6 to 9. Referring to FIGS. 6 to 9, it can be seen that, in Comparative Examples 1 to 4, the reflection rate with respect to the variation in the SOI layer thickness varied widely.

[0051]

Therefore, when the photolithography operation is performed on the SOI wafer having the buried insulator layer thickness not satisfying $(1/2)\times(\lambda/n)\times A$, the exposure state of the photoresist applied to the surface of the SOI wafer varies according to a position in a plane of the SOI layer when there is thickness distribution in the plane of the SOI layer, and this causes the difference in the developed resist pattern after exposure from the design pattern.

[0052]

It is to be noted that the present invention is not limited to the foregoing embodiment. The embodiment is just an exemplification, and any examples that have substantially the same feature and demonstrate the same functions and effects as those in the technical concept described in claims of the present invention are included in the technical scope of the present invention.

CLAIMS

1. A method for designing an SOI wafer that has an SOI layer formed on a buried insulator layer and is suitable for photolithography with an exposure light having a wavelength λ, the method comprising

designing a thickness of the buried insulator layer of the SOI wafer on the basis of the wavelength λ of the exposure light.

2. The method for designing an SOI wafer according to claim 1, wherein the thickness of the buried insulator layer of the SOI wafer is designed as a thickness d satisfying an expression $d=(1/2)\times(\lambda/n)\times A$, wherein d represents the thickness of the buried insulator layer, n represents a refractive index of the buried insulator layer, and A represents an arbitrary positive integer.

3. The method for designing an SOI wafer according to claim 1 or claim 2, wherein the buried insulator layer is any one of a silicon oxide film, a silicon nitride film, and a silicon oxynitride film, or a laminated insulator layer formed as a multilayer thereof.

4. A method for manufacturing an SOI wafer that has an SOI layer formed on a buried insulator layer and is suitable for photolithography with an exposure light having a wavelength λ, the method comprising the steps of:

designing a thickness of the buried insulator layer of the SOI wafer on the basis of the wavelength λ of the exposure light utilized for the photolithography that is to be performed on the SOI wafer after

manufacturing; and

fabricating the SOI wafer that has the SOI layer formed on the buried insulator layer having the designed thickness.

5. The method for manufacturing an SOI wafer according to claim 4, wherein the thickness of the buried insulator layer of the SOI wafer is designed as a thickness d satisfying an expression $d=(1/2)\times(\lambda/n)\times A$, wherein d represents the thickness of the buried insulator layer, n represents a refractive index of the buried insulator layer, and A represents an arbitrary positive integer.

6. The method for manufacturing an SOI wafer according to claim 4 or claim 5, wherein the buried insulator layer is any one of a silicon oxide film, a silicon nitride film, and a silicon oxynitride film, or a laminated insulator layer formed as a multilayer thereof.