INTEGRATED CIRCUIT PACKAGING SYSTEM WITH PAD CONNECTION AND METHOD OF MANUFACTURE THEREOF

TECHNICAL FIELD

The present invention relates generally to an integrated circuit packaging system, and more particularly to a system for an integrated circuit packaging system with connection.

BACKGROUND ART

Modern~~n~~ electronics, such as smart phones, personal digital assistants, location based services devices, enterprise class servers, or enterprise class storage arrays, are packing more integrated circuits into an ever-shrinking physical space with expectations for decreasing cost. Numerous technologies have been developed to meet these requirements. Some of the research and development strategies focus on new technologies while others focus on improving the existing and mature technologies. Research and development in the existing technologies can take a myriad of different directions.

Consumer electronics requirements demand more integrated circuits in an integrated circuit package while paradoxically providing less physical space in the system for the increased integrated circuits content. Continuous cost reduction is another requirement. Some technologies primarily focus on integrating more functions into each integrated circuit. Other technologies focus on stacking these integrated circuits into a single package. While these approaches provide more functions within an integrated circuit, they do not fully address the requirements for lower height, smaller space, and cost reduction.

One proven way to reduce cost is to use mature package technologies with existing manufacturing methods and equipments. Paradoxically, the reuse of existing manufacturing processes does not typically result in the reduction of package dimensions. The demand still continues for lower cost, smaller size and more functionality.

Thus, a need still remains for an integrated circuit packaging system including lower cost, smaller size, and more functionality. In view of the ever-increasing need to improve integration and cost reduction, it is increasingly critical that answers be found to these problems. In view of the ever-increasing commercial competitive pressures, along with growing consumer expectations and the diminishing opportunities for meaningful product

the inner pad 142 and the active side 148. The internal connector 150 can be directly on the inner pad 142.

The integrated circuit packaging system 100 can include the passivation 118 electrically isolating the interconnect structure 124 from another of the interconnect structure 124. The integrated circuit packaging system 100 can include a number of the outer pad 126 surrounding or outside a perimeter of the integrated circuit 144. The integrated circuit packaging system 100 can include a number of the inner pad 142 under the inactive side 146 of the integrated circuit 144. Multiple rows of leads 102 are outside the perimeter of the integrated circuit 144.

The integrated circuit packaging system 100 can include an encapsulation 152, which covers a semiconductor package to seal a semiconductor device providing mechanical and environmental protection. The encapsulation 152 can be formed over the passivation 118, the interconnect structure 124, the integrated circuit 144, and the internal connector 150. The encapsulation 152 can be formed covering the passivation top side 122, the interconnect structure 124, the integrated circuit 144, and the internal connector 150.

The encapsulation 152 can include an encapsulation non-horizontal side 154, which is a horizontal extent of the encapsulation 152. A plane of the encapsulation non-horizontal side 154 can be coplanar with a plane of a passivation non-horizontal side 156 of the passivation 118. The passivation non-horizontal side 156 is a horizontal extent of the passivation 118.

It has been discovered that the interconnect structure 124 connected to the lead 102 and the integrated circuit 144 enables flip chip integrated circuit (IC) packaging in a multi-row quad flat nonleaded (QFN) package that has not so far been done due to limitations in leadframe designs thereby fulfilling a need to efficiently configure a multi-row quad flat nonleaded (QFN) package for a flip chip device.

It has also been discovered that the interconnect structure 124 having the conductive trace 140 attached to the outer pad 126 and the inner pad 142 provides a solution that does not use bismaleimide triazine (BT) laminate frames to redistribute flip chip signals in a quad flat nonleaded (QFN) package with multi-row leads.

It has further been discovered that the interconnect structure 124 provides a low cost quad flat nonleaded (QFN) flip chip packaging methodology due to simpler substrate construction and layering, elimination of solder balls, and elimination of laminate usage compared to organic substrate products, standard ball grid array (BGA) laminates, and embedded wafer level ball grid array (eWLB).

What is claimed is:

1. A method of manufacture of an integrated circuit packaging system comprising:

forming ~~a lead~~ multiple rows of leads, one of the leads having a lead bottom side and a lead top side;

applying a passivation over the one of the leads with the lead top side exposed from the passivation;

forming an interconnect structure directly on the passivation and the lead top side, the interconnect structure having an inner pad and an outer pad with a recess above the lead top side, wherein the interconnect structure connects the inner pad to the outer pad and the outer pad is directly on the lead top side;

mounting an integrated circuit over the inner pad and the passivation, wherein the multiple rows of the leads are outside a perimeter of the integrated circuit; and

molding an encapsulation over the integrated circuit.

2. The method as claimed in claim 1 wherein forming the interconnect structure includes forming the interconnect structure having the outer pad with a non-vertical base directly on the lead top side.

3. The method as claimed in claim 1 wherein forming the interconnect structure includes forming the interconnect structure having a conductive trace attached to the inner pad and the outer pad.

4. The method as claimed in claim 1 wherein forming the multiple rows of the leads includes forming the one of the leads having a horizontal ridge between the lead bottom side and the lead top side.

5. The method as claimed in claim 1 further comprising forming a pillar having a pillar non-horizontal side facing a lead non-horizontal side of the one of the leads.

6. A method of manufacture of an integrated circuit packaging system comprising:

forming ~~a lead~~ multiple rows of leads, one of the leads having a lead bottom side and a lead top side;

applying a passivation over the one of the leads with the lead top side exposed from the passivation;

forming an interconnect structure directly on the passivation and the lead top side, the interconnect structure having an inner pad and an outer pad with a recess above the lead top side, wherein the interconnect structure connects the inner pad to the outer pad and the outer pad is directly on the lead top side;

mounting an integrated circuit over the inner pad and the passivation, wherein the multiple rows of the leads are outside a perimeter of the integrated circuit;

attaching an internal connector to the integrated circuit and the inner pad; and

molding an encapsulation over the integrated circuit.

7. The method as claimed in claim 6 wherein forming the interconnect structure includes forming the interconnect structure having a non-horizontal sidewall extending from a non-vertical base directly on the lead top side.

8. The method as claimed in claim 6 wherein forming the interconnect structure includes forming the interconnect structure having a conductive trace attached to and integral with the inner pad and the outer pad.

9. The method as claimed in claim 6 wherein:

forming the multiple rows of the leads includes forming the one of the leads having a horizontal ridge between the lead bottom side and the lead top side; and

applying the passivation includes applying the passivation directly on a ridge upper side of the horizontal ridge.

10. The method as claimed in claim 6 further comprising:

forming a pillar having a pillar top side and a pillar non-horizontal side facing a lead non-horizontal side of the one of the leads; and

wherein:

forming the interconnect structure includes forming the interconnect structure having the inner pad directly on the pillar top side.

11. An integrated circuit packaging system comprising:

~~a lead~~ multiple rows of leads, one of the leads having a lead bottom side and a lead top side;

a passivation over the one of the leads with the lead top side exposed from the passivation;

an interconnect structure directly on the passivation and the lead top side, the interconnect structure having an inner pad and an outer pad with a recess above the lead top side, wherein the interconnect structure connects the inner pad to the outer pad and the outer pad is directly on the lead top side;

an integrated circuit over the inner pad and the passivation, wherein the multiple rows of the leads are outside a perimeter of the integrated circuit; and

an encapsulation over the integrated circuit.

12. The system as claimed in claim 11 wherein the interconnect structure includes the outer pad with a non-vertical base directly on the lead top side.

13. The system as claimed in claim 11 wherein the interconnect structure includes a conductive trace attached to the inner pad and the outer pad.

14. The system as claimed in claim 11 wherein the one of the leads includes a horizontal ridge between the lead bottom side and the lead top side.

15. The system as claimed in claim 11 further comprising a pillar having a pillar non-horizontal side facing a lead non-horizontal side of the one of the leads.

16. The system as claimed in claim 11 further comprising an internal connector attached to the integrated circuit and the inner pad.

17. The system as claimed in claim 16 wherein the interconnect structure includes a non-horizontal sidewall extending from a non-vertical base directly on the lead top side.

18. The system as claimed in claim 16 wherein the interconnect structure includes a conductive trace attached to and integral with the inner pad and the outer pad.

19. The system as claimed in claim 16 wherein:

the one of the leads includes a horizontal ridge between the lead bottom side and the lead top side; and

the passivation is directly on a ridge upper side of the horizontal ridge.

20. The system as claimed in claim 16 further comprising:

a pillar having a pillar top side and a pillar non-horizontal side facing a lead non-horizontal side of the one of the leads; and

wherein:

the interconnect structure includes the inner pad directly on the pillar top side.