

"Acoustic monolithic power semiconductor
integrated circuit and acoustic system using the same".

The present invention relates to an acoustic monolithic power semiconductor integrated circuit and an acoustic system using the same.

5 An acoustic system to be carried on a vehicle such as an automobile may comprise front speakers and rear speakers. The sound volumes of the front and rear speakers can be so changed that the acoustic reproduction can be produced in a number of different ways e.g., mainly by the front speakers, mainly by the rear speakers, or by
10 both front and rear speakers in equal volumes when quadrophonic sound is required. According to one known method, the front and rear speakers are driven by output amplifiers which have their levels adjusted at their input sides and which are made independent of one
15 another. According to another known system, the front and rear speakers are connected with the output of one output amplifier through a plurality of level adjusting variable attenuators so that they may be driven. The sound volumes of the front and rear speakers can be varied by adjusting
20 the variable attenuators. The latter system has an advantage that the number of the output amplifiers can be minimized.

The abovementioned variable attenuators are, however, relatively expensive because they are required to admit

relatively high currents. In this case, moreover, a BTL (Balanced Transformer Less) amplifier is used as the output amplifier to increase the output power for an identical supply voltage, the variable attenuators have to be connected
5 with one pair of output terminals, respectively, with a view to adjusting the sound volumes of the front and rear speakers. For the stereophonic and quadrophonic acoustic reproduction, it is necessary that two sets of output amplifiers be used.

10 It is therefore an object of the present invention to provide an acoustic monolithic power semiconductor integrated circuit, which can be used for multiple purposes, and an acoustic system which is cheaper than the known systems referred to above.

15 According to the present invention there is provided an acoustic monolithic power semiconductor integrated circuit including:

(a) a first differential amplifier circuit for acoustic signal amplification having non-inverting and
20 inverting inputs directly connected to first and second input terminals of said integrated circuit, respectively:

(b) a first amplifier output circuit having a non-inverting input supplied with the output signal of said first differential amplifier circuit within said integrated
25 circuit and an inverting input connected to a first feedback terminal of said integrated circuit for determining the gain and output D.C. level of said first amplifier output circuit, said first amplifier circuit having its output terminal connected to a first output terminal of
30 said integrated circuit;

(c) a second differential amplifier circuit for acoustic signal amplification having non-inverting and inverting inputs directly connected to third and fourth input terminals of said integrated circuit, respectively;
35 and

(d) a second amplifier output circuit having a non-inverting input supplied with the output signal of said second differential amplifier circuit within said integrated circuit and an inverting input connected to a second feedback terminal of said integrated circuit for determining the gain and output D.C. level of said second amplifier output circuit, said second amplifier circuit having its output terminal connected to a second output terminal of said integrated circuit.

The present invention will now be described in greater detail by way of examples with reference to the accompanying drawings, wherein:-

Figure 1 shows a block diagram of one preferred form of an acoustic monolithic power semiconductor integrated circuit;

Figure 2 shows a four-amplifier and four-speaker acoustic system using two of the acoustic monolithic power semiconductor integrated circuits shown in Figure 1;

Figure 3 shows a detailed circuit diagram of the internal circuit diagram of the acoustic monolithic power semiconductor integrated circuit shown in Figure 1;

Figure 4 shows a circuit diagram in which the acoustic monolithic power semiconductor integrated circuits shown in Figure 1 are used for amplification of stereophonic two-channel signals; and

Figure 5 shows a circuit diagram in which the acoustic monolithic semiconductor integrated circuits shown in Figure 1 are used in a BTL amplifier.

referring first to Figure 1, the following circuits and external terminals are provided as the monolithic power semiconductor integrated circuit which corresponds to the portion enclosed by chain dotted lines.

There are provided two differential amplifier circuits 2a and 2b which have their outputs connected respectively to the non-inverting inputs (+) of amplifier output circuits 1a and 1b constituting the power semiconductor integrated circuit. The non-inverting inputs (+) and inverting inputs (-) of those differential amplifier circuits 2a and 2b are used as the input terminals $IN_1(+)$, $IN_1(-)$, $IN_2(+)$ and $IN_2(-)$ of the monolithic power semiconductor integrated circuit.

The inverting inputs (-) of the amplifier output circuits 1a and 1b are connected with external terminals FB_1 and FB_2 for constituting a feedback circuit. Moreover, the amplifier output circuits 1a and 1b have their outputs connected with the outputs OUT_1 and OUT_2 , respectively, thereby to provide supply terminals. The amplifier output circuits 1a and 1b also receive a supply voltage V_{cc} and an earth potential GND_1 .

The differential amplifier circuits 2a and 2b, which are located at the input portion of the monolithic power semiconductor integrated circuit comprise, as shown in Fig. 3, differential paired transistors Q_1 , Q_2 , Q'_1 and Q'_2 , load resistors R_3 and R'_3 , and constant current source transistors Q_5 and Q'_5 . A bias circuit is composed of a transistor Q_6 and a resistor R_4 . The base-emitter voltage of the transistor Q_6 having its collector

and base electrodes directly connected is applied to the base electrodes of the transistors Q_5 and Q'_5 so that a substantially preset constant current will flow through the transistors Q_5 and Q'_5 .

- 5 The base electrodes of the differential paired transistors Q_1 and Q'_1 are connected as the non-inverting terminals (+) of the differential amplifier circuits 2a and 2b with the external terminals P_1 and P_3 of the monolithic power semiconductor integrated circuit respectively.
- 10 The base electrodes of the other differential paired transistors Q_2 and Q'_2 are connected as the inverting input terminals (-) of the differential amplifier circuits 2a and 2b with the external terminals P_2 and P_4 of the monolithic power semiconductor integrated circuit,
- 15 respectively.

 The output signals of the differential amplifier circuits 2a and 2b are produced at the connections between the collector electrodes of the transistors Q_2 and Q'_2 and the load resistors R_3 and R'_3 , respectively.

- 20 A zener diode ZD, a resistor R_7 and a transistor Q_7 together constitute a constant voltage regulator. As a result, a substantially constant operating voltage is produced at the emitter of the transistor Q_7 independently of a voltage V_{cc} which is to be applied to the supply
- 25 voltage terminal P_9 of the monolithic power semiconductor

integrated circuit.

The amplifier output circuits 1a and 1b comprise as shown in Fig. 3, of modified type differential amplifier circuits, which consist of transistors Q_{10} , Q'_{10} , Q_{11} and Q'_{11} ,
5 and resistors R_9 and R'_9 , and first amplifier stages which comprise current mirror transistors Q_{12} , Q'_{12} , Q_{13} and Q'_{13} .

The base electrodes of the transistors Q_{10} and Q'_{10} of the first amplifier stage are supplied with the output signals of the differential amplifier circuits 2a and 2b
10 as the non-inverting inputs (+) of the amplifier output circuits 1a and 1b.

The first amplifier stage thus constructed are supplied with a substantially constant operating voltage from the above referred to constant voltage regulator through the
15 resistors R_5 and R_6 . The resistor R_5 has one of its ends connected through a terminal P_{13} with a supply voltage ripple eliminating filter capacitor so that the differential amplifier circuits 2a and 2b and the first amplifier stages can be operated with high stability.

20 The base electrodes of the transistors Q_{11} and Q'_{11} of the first amplifier stages are supplied with the output signals OUT_1 and OUT_2 of the output terminals P_5 and P_6 through D.C. and A.C. negative feedback circuits which ~~are~~ comprise resistors R_{11} , R'_{11} , R_{10} and R'_{10} , constant current
25 transistors Q_{14} and Q'_{14} and capacitors C_1 and C_2 connected with

negative feedback external terminals P_2 and P_8 . As a result, the A.C. voltage gains of the amplifier output circuits $1a$ and $1b$ are determined, and the output D.C. levels of the output terminals P_5 and P_6 are maintained at substantially half the level of the supply voltage V_{cc} .

The constant current transistors Q_{14} and Q'_{14} are biased by a bias circuit which comprises a resistor R_{18} and a transistor Q_8 .

The output signals of the first amplifier stages to be generated at the resistors R_9 and R'_9 are amplified by means of drive amplifier stages which comprise transistors Q_{15} , Q'_{15} , Q_{16} and Q'_{16} resistors R_{12} and R'_{12} , phase compensation capacitors C_{10} and C'_{10} , transistors Q_{17} and Q'_{17} and constant current load transistors Q_{18} and Q'_{18} . The pairs of transistors Q_{15} , Q_{16} and Q'_{15} , Q'_{16} are connected in Darlington configuration. The output signals of the drive amplifier stages thus constructed are fed both to the transistors Q_{20} , Q'_{20} , Q_{21} and Q'_{21} connected in Darlington configuration and to the transistors Q_{22} , Q'_{22} , Q_{23} and Q'_{23} connected in complementary configuration of the output amplifier stages.

The emitter electrodes of the transistors Q_{22} and Q'_{22} are connected with the idling current adjusting circuits, which comprise diodes D_1 to D_3 and D'_1 to D'_3 and

transistors Q_{24} and Q'_{24} , so that the crossover distortion of the output amplifier stages can be reduced.

A bootstrap capacitor C_{11} is connected between the output terminal P_5 and an external terminal P_{14} and a bootstrap capacitor C'_{11} is connected between the output terminal P_6 and an external terminal P_{15} .

The power semiconductor integrated circuit thus constructed can be used not only as a stereophonic two-channel system but also as a BTL system which is enabled to have a high output by using one of the amplifier circuits as a positive phase amplifier circuit and the other as a negative phase amplifier circuit, by supplying them with a common input, and by connecting a load between their both outputs.

Fig. 4 shows an embodiment, in which the power semiconductor integrated circuit is used for amplifying the stereophonic two-channel signals. The left and right channel signals L and R of the stereophonic two-channel signals are applied through input coupling capacitors C_{101} and C_{102} respectively, upon the external terminals P_1 and P_3 which are the non-inverting input terminals of the differential amplifier circuits 2a and 2b. Those external terminals P_1 and P_3 are earthed through resistors R_{101} and R_{102} , respectively, so that their D.C. levels can be maintained at the earth potential. On

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the other hand, the external terminals P_2 and P_4 which are the inverting input terminals of the differential amplifier circuits $2a$ and $2b$ are directly connected to earth.

Moreover, the external terminals P_5 and P_6 which are the
 5 output terminals of the amplifier output circuits $1a$ and $1b$ are connected through output coupling capacitors C_{103} and C_{104} with respective loudspeakers R_{L1} and R_{L2} . The loudspeaker R_{L1} is supplied with the left channel amplifier signals and the loudspeaker R_{L2} is supplied with the right
 10 channel amplifier signals.

Fig. 5 shows an embodiment, in which the power semiconductor integrated circuit is used in the BTL system. Monaural signals V_{in} are applied through the input coupling capacitor C_{101} to the external terminal P_1
 15 acting as the non-inverting input terminal of the differential amplifier circuit $2a$ and also to the external terminal P_4 acting as the inverting input terminal of the differential amplifier circuit $2b$. As a result, the output signals of both of the differential amplifier circuits $2a$
 20 and $2b$ are in opposite phases to each other. As a result, the loudspeaker R_L has its both ends connected directly with the output terminals of the amplifier output circuits $1a$ and $1b$, and is driven by the amplified monaural signals.

From the foregoing description, it will be understood
 25 that the power semiconductor integrated circuit can be

applied to the stereophonic two-channel signal amplification system and to the BTL system merely by a simple modification to the external circuit.

As shown in Fig. 2, the semiconductor integrated
5 circuit can also be used in a ^{four-amplifier and} four-speaker acoustic system. In this case, the fader control can be accomplished at the input, so that the cost of manufacture can be reduced.

In this embodiment circuit, a pair of two-channel power integrated circuits IC and IC' are used. A left
10 channel front loudspeaker LF is connected between the output terminals $P_5(OUT_1)$ and $P_6(OUT_2)$ of the power integrated circuit IC. A right channel front loudspeaker RF is connected between the output terminals $P'_5(OUT'_1)$ and $P'_6(OUT'_2)$ of the power integrated circuit IC'. A
15 left channel back loudspeaker LB is connected between the output terminal of $P_5(OUT_1)$ of the power integrated circuit IC and the output terminal $P'_5(OUT'_1)$ of the power integrated circuit IC'. Finally, a right channel back loudspeaker RB is connected between the output
20 terminal $P_6(OUT_2)$ of the power integrated circuit IC and the output terminal $P'_6(OUT'_2)$ of the power integrated circuit IC'.

There are associated with the input terminals of the
power integrated circuits IC and IC', ^{control} fader/circuits which

will now be described in greater detail.

The power integrated circuit IC has its input terminal $P_1(IN_{1(+)})$ supplied with the left channel input signals L and its other input terminal $P_2(IN_{1(-)})$ connected to earth. As a result, the amplifier circuits $2a$ and $1a$ are used as the positive phase amplifier output circuits.

On the other hand, the power integrated circuit IC' has its input terminal $P_4'(IN_{2(-)})$ supplied with the right channel input signals R and its other input terminal $P_3'(IN_{2(+)})$ connected to earth. As a result, the amplifier circuits $2'b$ and $1'b$ are used as the opposite phase amplifier output circuits.

Furthermore, the other amplifier circuits have their inputs supplied through fader control attenuators VR_1 to VR_4 with the following input signals.

The attenuators VR_1 to VR_4 are of a type in which part thereof is constituted by a conductor so that the attenuation is zero for a given angle of rotation. More specifically, the attenuators VR_1 and VR_4 consist of a conductor extending on one side to the fronts F from the centre points M, whereas the attenuators VR_2 and VR_3 consist of a conductor extending on one side to the backs B from the centre points M, the sliders of all four attenuators being gauged to rotate together.

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The power integrated circuit IC has its input terminal $P_4(IN_2(-))$ supplied with the left channel signals L through the attenuator VR_1 , which has its attenuation increased for rotational positions from the centre point M to the back B, and its input terminal $P_3(IN_2(+))$ supplied with the right channel signals R through the attenuator VR_3 which has its attenuation increased for rotational positions from the centre point M to the front F. As a result, the amplifier circuits 2b and 1b amplify the signals R-L at the centre points M of the attenuator VR_1 and VR_3 .

On the other hand, the power integrated circuit IC, has its input terminal $P_1'(IN_1(+))$ supplied with the right channel signals R through the attenuator VR_4 , which has its attenuation increased for rotational positions from the centre point M to the back B, and its input terminal $P_2'(IN_1(-))$ supplied with the left channel signals through the attenuator VR_2 which has its attenuation increased for rotational positions from the centre point M to the front F. As a result, the amplifier circuits 2'a and 1'a amplify the signals R-L at the centre points of the attenuators VR_2 and VR_4 .

The relationships between the rotational positions F, M and B of the attenuators VR_1 to VR_4 , the outputs of the respective amplifiers, and the inputs to the loudspeakers

of the acoustic system thus constructed are tabulated in Table 1 given below.

Table 1

VR	Output Signals of Each Amplifier				Signals of Each Speaker	
	P_5	P_6	P'_5	P'_6	LF	LB
	(1a)	(1b)	(1'a)	(1'b)	RF	RB
F	L	-L	R	-R	2L	L-R
					2R	R-L
M	L	R-L	R-L	-R	2L-R	2L-R
		$\left(\frac{R-L}{2}\right)$	$\left(\frac{R-L}{2}\right)$		$\left(\frac{3L-R}{2}\right)$	$\left(\frac{3L-R}{2}\right)$
B	L	R	-L	-R	2R-L	2R-L
					$\left(\frac{3R-L}{2}\right)$	$\left(\frac{3R-L}{2}\right)$
					L-R	2L
					R-L	2R

In Table 1, the reference letters F, M and B indicate the front, the centre point and the back of the attenuators VR_1 to VR_4 . The signals which are given in brackets in the last two columns in Table 1 indicate the case where the sliders of the move over the resistive

sections of the attenuators so that the attenuations are linearly varied in proportion to the angles of rotation of the attenuators VR_1 to VR_4 .

5 Since the fader control of the four-amplifier and four-speaker acoustic system can be accomplished at the input unit, such attenuators of small power and size which are not practical in known systems in which the fader control has been carried out at the output of high current flow, can be used so that the cost of manufacture
10 can be greatly reduced.

It should be understood that the above described power semiconductor integrated circuits are not limited to the foregoing embodiments but can be modified to include cases in which a two channel type circuit is used as the
15 power integrated circuit and in which a circuit having a differential amplifier circuit as its input unit is used as a one channel power integrated circuit.



CLAIMS.

1. An acoustic monolithic power semiconductor integrated circuit including:

(a) a first differential amplifier circuit for acoustic signal amplification having non-inverting and
5 inverting inputs directly connected to first and second input terminals of said integrated circuit, respectively;

(b) a first amplifier output circuit having a non-inverting input supplied with the output signal of said first differential amplifier circuit within said integrated
10 circuit and an inverting input connected to a first feedback terminal of said integrated circuit for determining the gain and output D.C. level of said first amplifier output circuit, said first amplifier circuit having its output terminal connected to a first output terminal of said
15 integrated circuit;

(c) a second differential amplifier circuit for acoustic signal amplification having non-inverting and inverting inputs directly connected to third and fourth input terminals of said integrated circuit, respectively; and

20 (d) a second amplifier output circuit having a non-inverting input supplied with the output signal of said second differential amplifier circuit within said integrated circuit and an inverting input connected to a second feedback terminal of said integrated circuit for
25 determining the gain and output D.C. level of said second amplifier output circuit, said second

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amplifier output circuit, said second amplifier circuit having its output terminal connected to a second output terminal of said integrated circuit.

2. An acoustic monolithic power semiconductor integrated circuit according to Claim 1, wherein the first input terminal is supplied with either the left or the right stereophonic signal and the third input terminal is supplied with the other stereophonic signal, and wherein the first output terminal is connected to a first loudspeaker and the second output terminal is connected to a second loudspeaker.

3. An acoustic monolithic power semiconductor integrated circuit according to Claim 1, wherein the first input terminal and the fourth input terminal are supplied with an input signal, and wherein a loudspeaker is connected between the first output terminal and the second output terminal.

4. An acoustic system comprising the first and second acoustic monolithic power semiconductor integrated circuits according to Claim 1, wherein the first acoustic monolithic power semiconductor integrated circuit has its first input terminal supplied with first channel input signal and its second input terminal supplied with a bias voltage, wherein said first acoustic monolithic power semiconductor integrated circuit has its fourth input terminal supplied with the first channel input signal through a first attenuator



and its third input terminal supplied with second channel
input signal through a third attenuator, wherein the
second acoustic monolithic power semiconductor integrated
circuit has its first input terminal supplied with the
5 second channel input signal through a fourth attenuator
and its second input terminal supplied with the first
channel input signal through a second attenuator,
wherein the second acoustic monolithic power semiconductor
integrated circuit has its fourth input terminal supplied
10 with the second channel input signal and its third
input terminal supplied with a bias voltage, and wherein
the first, second, third and fourth attenuators are
arranged so that the signal attenuations by the first
and fourth attenuators are reciprocal to those of the
15 second and third attenuators.

5. An acoustic system according to Claim 4,
wherein a first loudspeaker is connected between the
first and second output terminals of the first acoustic
monolithic power semiconductor integrated circuit,
20 wherein a second loudspeaker is connected between the
first output terminal of the first acoustic monolithic
power semiconductor integrated circuit and the first
output terminal of the second acoustic monolithic
power semiconductor integrated circuit, wherein a third
25 loudspeaker is connected between the first and second
output terminals of the second acoustic monolithic power
semiconductor integrated circuit, wherein a fourth



loudspeaker is connected between the second output terminal of the first acoustic monolithic power semiconductor integrated circuit and the second output terminal of the second acoustic monolithic power semiconductor integrated circuit, wherein the first and second
5 loudspeakers are used for the first channel signals whereas the third and fourth loudspeakers are used for the second channel signals.

6. An acoustic system according to Claim 5,
10 wherein the first and third loudspeakers are used as the front loudspeakers whereas the second and fourth loudspeakers are used for the rear loudspeakers in a quadrophonic system.

7. An acoustic system according to any one of
15 the preceding claims 4 to 6, wherein said first channel input signals are "left" signals and said second channel input signals are "right" signals in a stereophonic system.

8. An acoustic monolithic power semiconductor
20 integrated circuit according to any one of the preceding claims 1 to 3, wherein said inverting input of said first amplifier output circuit is connected to said first feedback terminal through a first feedback resistor formed in said integrated circuit and connected to
25 said output terminal of said first amplifier output circuit through a second feedback resistor formed in



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said integrated circuit, and wherein said inverting input of said second amplifier output circuit is connected to said second feedback terminal through a third feedback resistor formed in said integrated circuit and connected to said output terminal of said second amplifier output circuit through a fourth feedback resistor formed in said integrated circuit.

9. An acoustic monolithic power semiconductor integrated circuit constructed substantially as herein described with reference to and as illustrated in Figure 1; or Figure 4; or Figure 5 of the accompanying drawings.

10. An acoustic system utilizing a semiconductor integrated circuit constructed substantially as herein described with reference to and as illustrated in Figure 2 of the accompanying drawing.

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