A METHOD OF FORMING A LOW STRESS SILICIDE CONDUCTORS ON A SEMICONDUCTOR CHIP

ABSTRACT

A method of forming low resistivity conductive lines on a semiconductor substrate (12) is disclosed. In practicing the method a multichamber tool is used to advantage by forming a first doped polysilicon layer (14) on the surface of a substrate, forming a second undoped layer (16) on the doped layer, while maintaining the work piece in a first chamber (21) under a vacuum environment, moving the substrate to a second chamber (22) and thereafter forming a silicide containing layer (17) on the undoped polysilicon layer. Various techniques may be used to deposit either the polysilicon or the silicide layer such as sputtering may also be used. Practice of the method eliminates separation of silicide from polysilicon and increases product yield.

Figure 1.