CLAIMS

1. A semiconductor device package assembly, comprising:

a base component having a front side and a back side, the base component having a first metallization structure at the front side, and the first metallization structure being exposed in a contacting area at the front side;

a stack of semiconductor device dies, each semiconductor device die having a first side, a second side with a recess, and a second metallization structure having a contact pad at the first side and a contacting region exposed in the recess at the second side; and

metal bumps at least partially positioned in the recesses at the second sides of the semiconductor device die, wherein the metal bumps are electrically coupled to the contact pads of a second metallization structure of one semiconductor device die and a contacting region of an adjacent semiconductor device die , and wherein additional metal bumps are coupled to the contact pad of a lowermost one of the semiconductor device die and the first metallization structure of the based component;

wherein the semiconductor device dies are electrically coupled to each other and the base component via the first and second metallization structures without through-silicon vias, and wherein the first metallization structure and the second metallization structure have traces and vias without using a through-silicon via (TSV) extending directly from the first side to the second side of the semiconductor device stacked die.

2. The semiconductor device package assembly of claim 1, wherein the metal bumps extend from the contact pad of one semiconductor device to the contacting region of an adjacent semiconductor device across a distance of not more than 20 μm.

3. The semiconductor device package assembly of claim 1, wherein the metal bump is a center metal bump, and wherein the semiconductor device package assembly further comprises a side metal bump positioned at one side of the center metal bump.

4. The semiconductor device package assembly of claim 1, wherein a vertical dimension of the metal bumps is not more than 15 µm.

5. The semiconductor device package assembly of claim 1, wherein a vertical dimension of the metal bumps is about 10 µm.

6. The semiconductor device package assembly of claim 1, wherein at least one of the first metallization structure and the second metallization structure includes aluminum.

7. The semiconductor device package assembly of claim 1, wherein at least one of the first metallization structure and the second metallization structure includes copper.

8. The semiconductor device package assembly of claim 1, wherein the second metallization structure includes first, second and third metallization layers, and wherein the first metallization layer is electrically coupled to the metal bump.

9. The semiconductor device package assembly of claim 8, wherein the first metallization layer includes aluminum, and wherein the second metallization layer includes copper, and wherein the third metallization layer includes copper.

10. A semiconductor device stacked die assembly, comprising:

a first semiconductor device die having a front side and a back side, the semiconductor device die having a first metallization structure at the front side, the first metallization structure being exposed from the back side via a first recess;

a second semiconductor device die having a first side and a second side, the semiconductor device die having a second metallization structure at the first side, the second metallization structure being exposed from the second side via a second recess, the second recess being aligned with the first recess; and

a metal bump at least partially positioned in the first recess and electrically coupled to the second metallization structure and the first metallization structure wherein the first semiconductor device die is stacked directly on the second semiconductor device die and the first and second semiconductor device die are electrically coupled to each other without through-silicon vias, and wherein the first metallization

structure and the second metallization structure have traces and vias without using a through-silicon via (TSV) extending directly from the first side to the second side of the semiconductor device stacked die.

11. The semiconductor device stacked die assembly of claim 10, wherein the metal bump includes indium.

12. The semiconductor device stacked die assembly of claim 10, wherein the metal bump is a center metal bump, and wherein the semiconductor device stacked die assembly further comprises a side metal bump positioned at one side of the center metal bump.

13. The semiconductor device stacked die assembly of claim 10, wherein a vertical dimension is no more than 15 μm.

14. The semiconductor device stacked die assembly of claim 10, wherein a vertical dimension is about 10 μm.