SMALL VOLUME PROCESS CHAMBER WITH HOT INNER SURFACES

BACKGROUND OF THE INVENTION

1. Field of the Invention

[1] The present invention relates generally to etching semiconductor substrates, and more particularly, to systems and methods for plasma etching semiconductor substrates.

2. Description of the Related Art

[2] In general, the manufacturing of the integrated circuit devices (in the form of semiconductor substrates and wafers) includes the use of plasma etching chambers. The plasma etch chambers are capable of etching selected layers on the substrate as defined by a photoresist mask. The plasma etch chambers are configured to receive processing gases (i.e., etch chemistries) while a radio frequency (RF) power is applied to one or more electrodes of the plasma etch chamber. The pressure inside the plasma etch chamber is also controlled for the particular process. Upon applying the desired RF power to the electrode(s), the process gases in the chamber are activated such that a plasma is created. The plasma is thus configured to perform the desired etching of the selected layers of the semiconductor wafer.

[3] Low volatility byproducts are produced in some prior art plasma etch processes. By way of example, in a copper etch process using chlorine containing gases (e.g., Cl2 and HCl), the byproduct is CuClx. CuClx is non-volatile at room temperature. The low-volatility byproducts typically condense on the chamber walls. During each plasma etch cycle, the byproducts build-up on the chamber walls. Eventually the byproducts build-up to a certain thickness. The byproduct build-up then begins to "flake" off of the chamber walls and is therefore becomes a significant particle source. The particles can contaminate the substrates being etched in the chamber.

[4] Recognizing that the internal surfaces of the plasma etch chamber are exposed to the plasma, the chambers are often designed to permit the use of simple lining parts, such as,

disks, rings, and cylinders. Because these lining parts are configured to confine the plasma over the substrate being processed, these parts are continuously exposed and attacked by the processing plasma energies. Due to this exposure, these parts ultimately erode or accumulate polymer buildup, requiring replacement or thorough cleaning. However, the cleaning and/or replacement costs of these lining parts can become very expensive both in actual cost and in lost production time required for the cleaning and replacement.

[5] In view of the foregoing, there is a need for a system and method of substantially eliminating particle contamination from byproduct build-up on the walls of the plasma etch chamber.

SUMMARY OF THE INVENTION

[6] Broadly speaking, the present invention fills these needs by providing an improved system for processing a substrate. It should be appreciated that the present invention can be implemented in numerous ways, including as a process, an apparatus, a system, computer readable media, or a device. Several inventive embodiments of the present invention are described below.

[7] One embodiment includes a method of processing a substrate. The method including loading a substrate into a plasma chamber and setting a pressure of the plasma chamber to a pre-determined pressure set point. Multiple inner surfaces that define a plasma zone are heated to a processing temperature. A process gas is injected into the plasma zone to form a plasma and the substrate is processed. The processing temperature can be greater than about 200 degrees (e.g., between about 200 degrees C and about 400 degrees C or a higher temperature).

[8] The method further includes drawing a byproduct vapor from the plasma zone through a cold trap to condense the byproduct vapor in the cold trap. The cold trap has a temperature of at least about 50 degrees C cooler than the processing temperature.

[9] Processing the substrate can include etching the substrate. Processing the substrate can also include etching a copper film on the substrate. Heating the inner surfaces defining the plasma zone to the processing temperature can include maintaining a surface of the substrate at a second temperature sufficient to cause a byproduct vapor to condense on the

surface of the substrate to deposit a film on the substrate. The second temperature is about 50 degrees C cooler than the processing temperature.

[10] The pre-determined pressure set point is less than atmospheric pressure. The pre-determined pressure set point is within a range of about 1 mTorr and about 500 mTorr.

[11] The plasma chamber is a small volume plasma chamber. The small volume plasma chamber includes a first electrode. The first electrode forming a chuck for supporting the substrate. A second electrode is also included. The second electrode being deposed substantially parallel to the first electrode. The second electrode being one of the inner surfaces. The first electrode and second electrode being separated by a predetermined distance. The predetermined distance is equal to a range of between about 0.5 cm and about 5 cm. The small volume plasma chamber includes a hot liner, wherein the hot liner forms a portion of the plurality of inner surfaces.

[12] Processing the substrate includes a stress free planarization wherein the substrate is patterned, having a conductive interconnect material filling multiple features in the pattern. The conductive interconnect material having an overburden portion having at least one non-uniformity. The stress free planarization includes planarizing the overburden portion that includes depositing an additional layer on the overburden portion and planarizing the additional layer and the overburden portion. The additional layer being substantially entirely removed in the planarizing process.

[13] Another embodiment provides a small volume plasma chamber that includes a first electrode, the first electrode forming a chuck for supporting the substrate. A second electrode is also included. The second electrode being deposed substantially parallel to the first electrode. The first electrode and second electrode being separated by a predetermined distance. A hot liner is also included. The hot liner and the second electrode form a portion of several inner surfaces that define a plasma zone. The predetermined distance is equal to a range of between about 0.5 cm and about 5 cm.

[14] The small volume plasma chamber can also include a cold trap. The cold trap being sufficiently cooler than the inner surfaces that define the plasma zone to substantially cause a plasma byproduct vapor to condense in the cold trap. The cold trap is coupled to the plasma zone by a passage.

[15] Another embodiment provides a method of forming a semiconductor device including loading a patterned substrate into a plasma chamber. The substrate having a conductive interconnect material filling several features in the pattern. The conductive interconnect material having an overburden portion having at least one non-uniformity. A pressure of the plasma chamber is set to a pre-determined pressure set point. Multiple inner surfaces that define a plasma zone, are heated to a processing temperature of greater than about 200 degree C. A process gas is injected into the plasma zone to form a plasma. The substrate is processed which includes forming an additional layer on the overburden portion and planarizing the additional layer and the overburden portion. The additional layer being substantially entirely removed in the planarizing process. A byproduct vapor from the plasma zone is drawn through a cold trap to cause the byproduct vapor to condense in the cold trap. The conductive interconnect material can include copper.

[16] The present invention provides a small volume plasma chamber having multiple inner surfaces capable of being substantially uniformly heated to a processing temperature to ensure that byproduct vapors, especially byproduct vapors having a low volatility, will not condense on the inner surfaces so as to form particle contamination sources.

[17] Further, the byproduct vapors are drawn away from the plasma zone and through a cold trap where the byproduct vapors can condense. The cold trap is sufficiently physically isolated that particles formed by the condensed byproduct vapors are substantially prevented from migrating to the substrate being processed.

[18] The present invention provides an advantage of substantially minimizing the particle generation and resulting substrate contamination. This is achieved by substantially eliminating condensation of plasma chemistries on the inner surfaces of the plasma chamber. Condensation is directed in a cold trap that is at least partially physically isolated from the plasma zone.

[19] Other aspects and advantages of the invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[20] The present invention will be readily understood by the following detailed description in conjunction with the accompanying drawings, and like reference numerals designate like structural elements.

[21] Figure 1A shows side view of a small volume plasma etch process chamber, in accordance with one embodiment of the present invention.

[22] Figure 1B is a flowchart of the method operations for etching a substrate in the plasma chamber described above, in accordance with one embodiment of the present invention.

[23] Figure 2A shows a patterned semiconductor substrate in a dual damascene process in accordance with one embodiment of the present invention.

[24] Figure 2B shows an additional layer added in accordance with one embodiment of the present invention.

[25] Figure 3 shows a substantially planar overburden portion in accordance with one embodiment of the present invention.

[26] Figure 4A shows the substrate having undergone a second etching process in accordance with one embodiment of the present invention.

[27] Figure 4B shows the substrate having undergone a barrier removal process in accordance with one embodiment of the present invention.

[28] Figure 5 is a flowchart of the method operations of performing a local planarization, in accordance with one embodiment of the present invention.

[29] Figures 6A-6D show a sequence of chemical conversion and etch-back processes applied to a substrate to increase local uniformity, in accordance with one embodiment of the present invention.

[30] Figure 7 is a flowchart of the method operations of the chemical conversion and etch-back processes applied to a substrate to increase local uniformity, in accordance with one embodiment of the present invention

[31] Figure 8 is a flowchart of the method operation of correcting global non-uniformities in accordance with one embodiment of the present invention.

[32] Figure 9 shows a substantially removed, planarized overburden portion in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

[33] Several exemplary embodiments for an improved system and method for performing a plasma etch process on a substrate will now be described. It will be apparent to those skilled in the art that the present invention may be practiced without some or all of the specific details set forth herein.

[34] One embodiment provides a plasma etch chamber with a relatively small volume that includes a capacitively coupled RF source. The inner surface area of the small volume plasma etch chamber is sufficiently small that the inner surface area can be easily heated to an elevated temperature (e.g., greater than about 200 degrees C). The elevated temperature is sufficient to substantially prevent a low volatility byproduct from condensing on the inner surface. The capacitively coupled RF plasma chamber uses parallel plates having a narrow gap between them. The parallel plates form a top and bottom electrodes with the substrate situated on the bottom electrode and the top electrode situated very close to the surface of the substrate. In this configuration, the top and bottom electrodes form a majority of the inner surface area.

[35] Figure 1A shows side view of a small volume plasma etch process chamber 100, in accordance with one embodiment of the present invention. A substrate 108 being processed is clamped to a heated chuck 102 that also serves as the bottom electrode. The chuck 102 can be an electro-static chuck. A focus ring 122 can also be included in the bottom electrode.

[36] Process gases are delivered from a gas source trough an inlet port 126. The process gases flow through an optional baffle plate 106 and through a perforated "showerhead-type" top electrode 104. The baffle plate 106 disperses the gas flow. The baffle plate 106 can be separated from the top electrode 104 by a low contact dielectric 116 (e.g., quartz, insulator, etc.) so that the baffle plate 106 is not substantially connected to the tope electrode 104 either electrically or thermally. A plasma zone 114 is formed by the volume defined by the top electrode 104, the bottom electrode 102 and the hot liner 124. The gas flow is well dispersed in the plasma zone 114.

[37] The top electrode 104 and the bottom electrode 102 are separated by a distance d of about 0.5 cm to about 5 cm. In one exemplary embodiment, d is equal to about 2 cm. The top electrode 104 can be coupled to a ground potential 112 and the bottom electrode 102 coupled to the RF source 110 as shown. In an alternative embodiment, the bottom electrode 102 can be coupled to the ground potential 112 and the top electrode 104 coupled the RF source 110. The RF source can have a frequency of between about 400 kHz and about 60 MHz. The RF source can have a voltage of between about 100 volts and about 2000 volts.

[38] In an alternative embodiment, the plasma chamber 100 can be configured in a push-pull configuration. In the push-pull configuration, both the top electrode 104 and the bottom electrode 102 are powered by the RF source. The sputtering from ions in the push-pull configuration can further reduce the deposition of the low-volatile by-products on the top electrode 104. As described above, the deposition of etch by-products on the top electrode 104 is a major concern since it is proximate to the surface substrate 108. The push-pull configuration plasma chamber 100 can also be powered from a single RF source 110. In this push-pull RF configuration, the plasma potential is reduced to one half, which allows the plasma to be more easily confined in the plasma zone 114.

[39] The process gases can be heated by hot plasma bombardment. If a higher temperature is needed to prevent deposition of the byproducts on the inner surface area, then additional electric heaters can be embedded in the top electrode 104. A hot liner 124 between the electrodes is electrically heated to prevent any deposition on the liner. The hot liner 124 can be heated with embedded resistive heaters or other types of heat sources (e.g., hot oil, radiant heat source) The hot liner 124 can also serve as a plasma confinement barrier defining a plasma zone 114 formed between the top electrode 104, the bottom electrode 102 and the hot liner. The hot liner 124 can be manufactured from a plasma resistant material (e.g., quartz or alumina or any suitable materials coated with plasma resistant layers).

[40] In an exemplary use, a copper film can be etched using a chlorine containing gaseous species. In such a use, the minimum temperature for all surfaces (e.g., hot liner 124, top electrode 104, and bottom electrode 102) that are around the substrate 108, should be between about 200 to about 400 degrees C. At that temperature range the etch byproducts (e.g., CuClx) and other chemistries in the plasma are vaporized at a sufficient vapor pressure

and can therefore be pumped out of the plasma zone 114 in the plasma etch chamber and out of the outlet ports 116. As the temperature is increased, the volatility of the various chemistries and byproducts in the plasma also increases. As a result, vapors having a low volatility (e.g., copper etch byproducts) can be more efficiently evacuated from the plasma zone 114 as the temperature is increased. Because the low volatility copper etch byproducts are more effectively evacuated, then the particle generation caused by build-up of the etch byproduct on the inner surfaces of the plasma zone 114 is substantially reduced.

[41] It should be understood that while 400 degrees C is cited herein is an exemplary upper temperature limit, the chamber is not limited to 400 degrees C and could be heated to a much higher temperature if desired. By way of example, if a particular etch by product did not have a sufficient vapor pressure until heated to 500 degrees C, then the process chamber could be sufficiently heated to 500 degrees C. Temperatures higher than 500 degrees C can also be used.

[42] In contrast, a typical prior art plasma etch chamber is too large to be effectively heated to 200 degrees C and at least some portion of the inner surface of the prior art plasma etch chamber is sufficiently cool enough that the etch byproducts can condense and eventually build-up and flake off, thereby becoming a particle contamination source. The typical plasma etch processes occur at less than 100 degrees C (e.g., 60 degrees C) and as described above, the etch byproducts can condense on the inner surfaces, near the substrate, and cause particle contamination.

[43] Because the etch byproduct CuClx has a low volatility, the plasma etch process can be accomplished at a pressure less than or equal to about atmospheric pressure (i.e. less than or equal to about 1 Torr). By way of example the copper plasma etch process can be operated at a range of about 1-500 mTorr.

[44] A cold trap 120 is included adjacent to the hot liner 124. A narrow passage 126 through the hot liner 124 couples the plasma zone 114 with the cold trap 120. As gases and the etch byproduct vapor is pumped out of the plasma zone 114, the etch byproduct vapor is drawn through the cold trap 120 and drawn out the outlet ports 116 by one or more pumps 144. Much of the etch byproduct condenses in the cold trap 120. As a result, the etch byproduct gradually builds up on the surfaces of the cold trap 120. Any particles (e.g., flakes

and other loose etch byproduct buildup) that form in the cold trap 120 cannot easily migrate back to the plasma zone 114, and therefore to the substrate 108, due to the relatively small width of the narrow passage 126. By way of example, the narrow passage 126 can have a width of between about 5mm to about 20mm. In this manner the particles are sufficiently physically separated from the substrate 108 to substantially eliminate particle contamination resulting from the plasma etch byproducts.

[45] The cold trap 120 can be actively cooled or may simply not be heated and therefore sufficiently cool to cause the etch byproducts to condense. The cold trap 120 can be thermally isolated from the heated portions of the plasma chamber 100 so that the cold trap will remain substantially cooler than the heated portions (e.g., more than about 50 degrees C cooler, for example, than the hot liner 120 and the substrate 108). By way of example the cold trap 120 can be thermally coupled to the wall of the chamber 100 or the chuck housing 142 so that the cold trap 120 will remain approximately the same temperature as the respective wall of the chamber 100 or the chuck housing 142.

[46] The substrate 108 can be loaded in to the plasma etch chamber 100 via a loading port 128. The bottom electrode 1-2 can be lowered in the chuck housing 142 or the hot liner 124 can be lifted (e.g., by lifters 130) or combinations thereof to provide substrate loading and unloading access to the plasma zone 114.

[47] Figure 1B is a flowchart of the method operations 150 for etching a substrate in the plasma chamber 100 described above, in accordance with one embodiment of the present invention. In an operation 155, the substrate is loaded into the plasma chamber 100 (e.g., through the loading port 128). The loading port can also be closed for processing. In an operation 160, a pressure inside the plasma chamber 100 is adjusted to the desired set point as described above.

[48] In an operation 165, the plasma chamber 100 is heated to the required processing temperature. The processing temperature can be any temperature sufficiently high enough to provide sufficient volatility of the desired species. As described above, in a copper etch process using a chlorine containing gaseous etchant species, the processing temperature is about 200 degrees C or even higher (e.g., about 250 to about 400 degrees C). If the intended process is an etch process, then all inner surfaces exposed to the plasma zone 114 are heated

to the processing temperature. In the alternative, if the intended process is a deposition process, then all inner surfaces exposed to the plasma zone 114, except the substrate 108, are heated to the processing temperature. Heating the inner surfaces to the processing temperature can be accomplished by forming a plasma in the plasma zone 114 or by actively heating the various surfaces with resistive, radiant or other types of thermal energy sources.

[49] In an operation 170, the process gases are injected into the plasma chamber 100 and a etch (or deposition) plasma is formed. In an operation 175, the etching (or deposition) operation is performed. In an etching operation, the etching chemistry etches away a portion of the surface of the substrate 108 that is exposed to the plasma. By way of example, a copper layer can be etched by a chlorine containing species causing CuClx byproducts to be vaporized in the plasma.

[50] In an operation 180, the byproduct vapors and gases are drawn out of the plasma zone 114 and through the cold trap 120 and out of the plasma chamber 100 by the pump(s) 144. At least a portion of the byproduct vapors condense on the relatively cool surfaces of the cold trap 120, as the byproduct vapors are drawn through the cold trap. In this manner substantially all of the particles that may be caused by the condensed byproduct vapors are formed away from the inner surfaces that the substrate 108 is exposed to. As a result, the particle contamination of the substrate 108 is substantially eliminated.

[51] In an operation 185, the etching (or deposition) operation is ended. The etching (or deposition) operation ends when a desired result is achieved. By way of example, the operation ends when an etching time has been achieved or when a desired end point has been achieved. In an operation 240, the substrate 108 is removed from the plasma chamber 100 and the method operations end.

[52] While the above examples are described in terms of copper etch processes with chlorine based etchants, the present invention is not limited to copper etches. By way of example a platinum material could be etched by chlorine and carbon monoxide gases. Other etchant species can include HBr, HI, BCl_3 and CF_4.

[53] In an alternative embodiment, the chamber 100 shown in Figure 1A can also be used to perform chemical vapor deposition (CVD). In a CVD operation, the chuck 102 may be cooled heated so that the vapor species will deposit on the substrate 108 mounted on the

chuck 102. By way of example, an organic film can be deposited using C_2H_4 or C_2H_2 as precursors. In another CVD embodiment, a copper film can be deposited either thermally or using plasma assistance on the substrate 108 and inner surfaces. After the substrate 108 is removed from the processing chamber, the copper film on hot inner surface can be cleaned using a chlorine or a bromine containing etchant. The plasma chamber 100 can be used to perform a stress free planarization or any other plasma process application.

[54] Figure 2A shows a patterned semiconductor substrate 200 in a dual damascene process in accordance with one embodiment of the present invention. The substrate 200 has been patterned as part of the semiconductor manufacturing process such as a dual damascene manufacturing process. A mask can be used to pattern the substrate 200. The substrate 200 includes a large, somewhat isolated feature 202 (e.g., trench, via, etc.) a smaller, somewhat isolated feature 204 and several features 206 that are densely packed together. A barrier layer 210 is also included. The barrier layer 210 is typically a different material than the substrate 200 or a conductive interconnect material 220. The conductive interconnect material 220 can be copper or copper alloy or other conductive material.

[55] An overburden portion 212 of the conductive interconnect material 220 extends above the features 202, 204, 206 and includes corresponding localized variations 214, 216, 218 in thickness of the overburden portion 212. As shown, the larger feature 202 has a corresponding larger decrease in the thickness of the overburden portion 212 as compared to the smaller feature 204, which has a slightly smaller variation in thickness of the overburden portion 212. The densely packed features 206 have a somewhat increased thickness of the overburden portion 212.

[56] Typical etch processes etch the overburden portion 212 of the conductive interconnect material 220 at a fairly uniform rate over the entire wafer area and therefore the typical etching process will expose the barrier layer 210 near the large feature 202 before the barrier layer 210 near the densely packed features 206 will be exposed. In sum, the typical etching process cannot planarize the overburden portion 212 of the conductive interconnect material.

[57] Figure 2B shows an additional layer 222 added in accordance with one embodiment of the present invention. The additional layer 222 is formed on top of the overburden portion

212. The additional layer 222 can be a substantially planar fill material (e.g., spin on glass (SOG), polysilicon, polymer resist, bilayer, UV or thermally curable material, or other material that can flow to form a planar surface and which has the appropriate etching characteristics). An optional, relatively thin (e.g., about 25-100 nm in thickness) conformal layer 224 may also be included between the additional layer 222 and the overburden portion 212. The conformal layer 224 can be a barrier layer or an adhesion layer. The conformal layer 224 can allow a wider variety of materials that can be used for the additional layer 222.

[58] The additional layer 222 and the overburden portion 212 have a substantially 1:1 etch selectivity so that a subsequent etching process (e.g., plasma or gaseous etch process) can etch both the additional layer 222 and the overburden portion 212 at substantially the same rate.

[59] Figure 3 shows a substantially planar overburden portion 212' in accordance with one embodiment of the present invention. Because the additional layer 202 forms a substantially planar surface over the stack of layers 200, 210, 212, 222, a first etching process can uniformly etch the additional layer 222 and the overburden 212 over the entire area until the remaining overburden portion 212' is substantially locally planar in that the local variations 214, 216, 218 are substantially eliminated.

[60] A typical recipe would involve conditions that provide a 1:1 etch selectivity between the additional layer 222 and the overburden portion 212. By way of example, if the additional layer 222 is SOG, and the overburden portion 212 is copper, then a halogen (e.g., Cl, F, Br, I) based chemistry provides etch rate control for both the SOG as well as copper to allow for tuning for the desired 1:1 selectivity. Although any plasma feed gas producing reactive halogen radicals can be used, CF4, Cl2, and HCl are typical examples. Various process parameters can be adjusted to control etch rates, selectivity, uniformity and reduce corrosion include variation of process variables such as substrate temperature and inclusion of one or more additives (e.g., Ar, H2, Cl, O2, CH3X (X = F, Cl, Br, I), CH2F2, and CH4).

[61] Another approach involves a sputter dominant etch with Ar or other inert gas such as He, Xe, Ne, Kr, as the primary etchant of the copper overburden portion 212 with other additives to provide etch rate control of the additional layer 222 and passivation of the top surface of the remaining copper 212. The other additives can include, for example H2 and/or

CF4. Either of these processes is can operate over a wide temperature range of between about 75 degrees C and about 400 degrees C.

[62] The first etching process is an etch process designed to leave the remaining overburden portion 212' substantially locally planar in that the local variations 214, 216, 218 are substantially eliminated. One or more subsequent etching processes will remove the bulk or the majority of the overburden portion 212'. A finish etching process can be applied to continue the etching process to an endpoint at which the overburden portion 212' is removed from the barrier 210. The finish etching process can also be included in the bulk etch process. Subsequent processes after the finish etch can include selective barrier removal and passivating the remaining conductive material 220 to prevent corrosion and provide stability for further processing. An additional operation after the finish etch can be designed not to significantly remove any material but only passivate the remaining conductive material 220 to prevent corrosion and provide stability for further processing.

[63] Figure 4A shows the substrate 200 having undergone a second etching process in accordance with one embodiment of the present invention. The second etching process continues to an endpoint such that the barrier layer 210 will be exposed at all locations substantially simultaneously and leaving only the portion 220 of the conductive material (e.g., copper, copper-containing alloys and combinations, and other conductive material) that fills the features 202, 204, 206.

[64] The first etching process and the second etching process can be substantially similar or significantly different. By way of example, the first etching process can be an etching process for improving the local planarity of the overburden portion 212 due to local non-uniformities 214, 216, 218 (e.g., caused by feature 202, 204, 206 locations, sizes and concentrations in underlying layers). The entire additional layer 222 and a portion of the overburden portion 212 can be removed in the first etching process. By comparison, the second etching process can be a much more selective etching process that removes the bulk of the remaining, planar overburden 212' to the endpoint (i.e., when the barrier layer 210 is exposed).

[65] Figure 4B shows the substrate having undergone a barrier removal process in accordance with one embodiment of the present invention. A portion of the barrier layer 210

is removed to expose an underlying mask layer 402. Only the portion of the barrier layer 210 that is formed within the features 202, 204, 206 remain. A typical second etching process removes the bulk portion of the overburden 212 at high rate and preferably with a high selectivity to the barrier layer 210. By way of example, if the overburden portion 212 is copper, a halogen - based chemistry (e.g., Cl2, CF4, HCl, HBr, BCl3) can be effectively used for the second etching process. In another approach a physically dominant etch process such as an Ar (or other noble or inert gas) based sputter process can be used. Various process parameters can be adjusted to control etch rates and selectivity. The various process parameters can include adjusting process variables such as substrate temperature balance of reactive species, and inclusion of one or more additives (e.g., H2, O2, Ar, He, Xe, Ne, Kr, etc.).

[66] Figure 5 is a flowchart 500 of the method operations of performing a local planarization, in accordance with one embodiment of the present invention. In operation 505, the additional layer 222 is added on top of the conductive overburden portion 212. In operation 510, the first etch process is applied to remove the majority of the additional layer 222 and the conductive overburden portion 212. In operation 515, the second etch process is applied to remove the remaining overburden portion 212' to the endpoint.

[67] In an alternative embodiment, operation 515 can also include a finish etch process as described above. Subsequent processes after the finish etch can include selective barrier removal and passivating the remaining conductive material 120 to prevent corrosion and provide stability for further processing. An additional operation after the finish etch process can be designed not to significantly remove any material but only passivate the remaining conductive material 220 to prevent corrosion and provide stability for further processing.

[68] Figures 6A-6D show a sequence of chemical conversion and etch-back processes applied to a substrate 600 to increase local uniformity, in accordance with one embodiment of the present invention. Figure 7 is a flowchart 700 of the method operations of the chemical conversion and etch-back processes applied to a substrate 600 to increase local uniformity, in accordance with one embodiment of the present invention. As shown in Figure 6A, the substrate 600 has a substantially non-planar overburden portion 602 with non-planar surface profile 606, similar to the substrate 100 described in Figure 2A above.

[69] Referring now to Figures 6B and 7, in operation 705, an additional layer 604 is formed on top of the overburden portion 602. The additional layer 604 may be deposited or formed on the overburden portion 602. By way of example, the additional layer 604 can be formed through a chemical conversion of a top-most portion of the overburden portion 602. If the overburden portion 602 is copper or copper alloy, then a controlled exposure to a gas can form a copper reaction product layer 604. One example is a halogen gas that can form a Cu-halide layer 604. The copper reactant layer 604 diffuses into the surface of the copper overburden 602 to convert a top portion of the copper overburden 602. Processes for chemical conversion of copper are known in the art, such as Nagraj S. Kulkarni and Robert T. DeHoff, "Application of Volatility Diagrams for Low Temperature, Dry Etching, and Planarization of Copper", Journal of Electrochemical Society, 149 (11) G620-G632, 2002.

[70] In another example, the additional layer 604 can be deposited on the overburden portion 602. The deposited layer 604 can include a polymer layer or an oxide layer being deposited on the overburden portion 602.

[71] Referring now to operation 710 and Figure 6C, an etch-back process is applied to remove the additional layer 604. A portion of the overburden portion 602 may also be removed. Removing the additional layer 604 results in further softening (i.e., planarizing) of the profile of the overburden portion 602 to profile 606'. The Cu-halide substantially softens the contours of the overburden portion 602. A Cu-halide can also maintain a substantially 1:1 etch-back selectivity with the copper overburden portion 602. Operations 705 and 710 can be repeated multiple times to substantially planarize the overburden portion 602 to subsequent profiles 606' and 606'', as shown in Figure 6D, until the resulting profile is substantially planar.

[72] Chemical conversion of copper overburden portion 602 utilizing shape dependence of compound formation can be typically achieved by oxidizing the copper at the Cu-reactive species interface. Copper oxidization in this instance can include a chemical conversion of elemental copper to a copper compound with copper in a positive oxidation state. By way of example, oxidation of the copper to cuprous- or cupric chloride (CuCl or CuCl2) at the surface can occur in a chlorine plasma at lower temperatures (e.g., < 200 degrees C).

[73] The etch-back process involves reduction of this copper compound to another chemical compound capable of being volatile and thus leaving the surface of the remaining overburden 602' at the fixed substrate temperature. By way of example, there can be a reduction of the CuCl2 to volatile Cu3Cl3 in the presence of reactive hydrogen species (e.g., H2 plasma). Alternating the shape-dependent conversion followed by etch-back of the converted portion can lead to bulk removal of the copper overburden portion 602, while simultaneously planarizing the topography (e.g., profile) of the copper overburden 602.

[74] In operation 715, if the overburden portion 602 is substantially planarized, then the method operations end. Alternatively, if in operation 715, the overburden portion 602 is not substantially planarized, then the method operations continue at operation 705 above. In one embodiment, operations 705-715 can occur in situ within a single etch chamber. In an alternative embodiment, operation 710 can occur ex situ and can include ECD or low-down force CMP processes to achieve the substantially planar overburden portion 602' as shown in Figure 6D.

[75] The method operations described in Figures 6A-7 can be used as a planar bulk removal process that performs both planarization of the non-planar overburden portion 602 and removal of the bulk of the overburden portion 602.

[76] The local planarization of the substrates 200, 600 can be determined through any one or more of several known layer thickness mapping technologies that are known in the art. By way of example, an eddy current sensor can map the thickness of the overburden portion 212, 212' as described in commonly owned U.S. Patent Application 10/328,912 entitled System, Method And Apparatus For Thin-Film Substrate Signal Separation Using Eddy Current by Gotkis et al., filed on December 23, 2002 and U.S. Patent Application 10/251,033 entitled System And Method For Metal Residue Detection And Mapping Within A Multi-Step Sequence by Gotkis et al., filed on September 19, 2002, which are incorporated by reference herein, in their entirety.

[77] The methods and systems described in Figures 2A-7 above describe various approaches to substantially eliminating local, pattern dependant non-uniformities in an overburden portion. However, methods and systems described in Figures 2A-7 above do not directly address correction of global non-uniformities. Global non-uniformities can include

variations in removal rates of material in the center of the substrate as compared to the edge of the substrate and other non-uniformities that are not localized phenomena.

[78] Figure 8 is a flowchart of the method operation 800 of correcting global non-uniformities in accordance with one embodiment of the present invention. In operation 805, a substrate having localized non-uniformities such as feature-pattern dependant non-uniformities in the overburden portion is received. In operation 810, the localized non-uniformities are substantially eliminated such as through CMP, ECP or the methods and systems described in Figures 2A-7 above or any other method known in the art. Substantially removing the localized non-uniformities forms a substantially, locally planarized overburden portion such as the planarized overburden portion 212' shown in Figure 3 above.

[79] Figure 9 shows a substantially removed, planarized overburden portion 902 in accordance with one embodiment of the present invention. The substantially removed, planarized overburden portion 902 can be a relatively thin overburden portion such as a few hundred angstroms in thickness.

[80] In operation 815, the substrate with the planarized overburden portion is mapped to identify and quantify any global non-uniformities in the planarized overburden portion. The planarized overburden portion can be mapped with any one or more of several known layer thickness mapping technologies that are known in the art as described above. The mapping can be in situ (within the current process chamber) or ex situ (external to the current process chamber). An in situ mapping process can also be dynamic and allow for the subsequent processes to be dynamically adjusted as the subsequent processes progress.

[81] In operation 820, the location and quantity of the global non-uniformities, as determined in operation 815 above, are removed in a substantially mechanical stress-free process by adjusting an etching process to address the specific requirements of the detected global non-uniformities in a finish etch process. By way of example, if the remaining overburden portion 902 were approximately 500 angstroms thick in the center and 300 angstroms thick on the edge, then the recipe can be adjusted such that the center to edge non-uniformity can be compensated for so that the entire barrier layer 210 will be exposed

simultaneously. The stress-free process avoids the CMP problems described above because no mechanical force is applied to the substrate during the etch-back process.

[82] The recipe (e.g., selected values of process variables) that is selected is selective to barrier layer 210 (i.e., will etch the barrier at a much slower rate than the recipe will etch the copper, e.g., a typical selectivity range of copper etch over barrier etch in these processes is greater than about 1 but less than about 3) and that will minimize any recesses (e.g., excess removal of the conductive material 120 in the features 202, 204, 206).

[83] The finish etch can have relatively slow etch rates for both copper of the remaining overburden portion 902 and the barrier layer 210 to minimize any recess into the features 202, 204, 206 with respect to the remaining height barrier of the barrier layer 210. As a result, the finish etch cannot have a very high selectivity to etch the copper.

[84] A final etch-back process can also be included. The final etch-back process includes etch-back of the mask material and/or the ILD material with appropriate selectivity and uniformity control such that the final outcome provides substantially globally uniform and substantially planar features with minimal copper and ILD loss (e.g., any copper recess is globally uniform across the substrate 200 at the end of the final etch and barrier removal processes). In this instance, the final etch would include a uniform process to etch-back the mask material with high selectivity to minimize copper loss and minimize the copper recess. By way of example, a halogen-based process where the halogen concentration is low and the substrate temperature is low (e.g., less than about 200 degrees C) will maintain a low copper etch rate while still sufficiently chemically etching the mask material. Any plasma feed gas including halogen reactive species (e.g., CF4, C2F6, C4F6) can be used. Etch rate control additives can include Ar, O2, CH2F2 and others can also be included.

[85] If the global copper recess and/or mask/ILD loss are non-uniform across the substrate at the end of the finish etch and final etch-back process, then additional variations in the recipe must be taken to correct for the global non-uniformities. By way of example, typical instances are a result of etch non-uniformity are described as center fast or edge fast etch rates. In either of these instances, can result in a variation in copper recess and/or mask/ILD loss across the substrate. Compensation can be achieved to counter this variation to obtain globally planar features with minimal copper and mask loss utilizing appropriate uniformity

and selectivity controls during the final etch-back of the mask/ILD material. In the instance of a center-fast finish etch process resulting in larger copper recess in the center of the substrate can be compensated for by an edge-fast final etch back process which selectively etches the mask material to bring to the same level as the copper level in the features 202, 204, 206. Typical selectivity obtained in this process is greater than about 2. Variations of the recipe to provide for uniformity control include pressure, temperature variation across substrate, ion flux uniformity controls, gas concentrations and chamber wall temperature. Variations to control selectivity include reactive halogen species concentration, substrate temperature, and bias power.

[86] Any of the operations described herein that form part of the invention are useful machine operations. The invention also relates to a device or an apparatus for performing these operations. The apparatus may be specially constructed for the required purposes, or it may be a general-purpose computer selectively activated or configured by a computer program stored in the computer. In particular, various general-purpose machines may be used with computer programs written in accordance with the teachings herein, or it may be more convenient to construct a more specialized apparatus to perform the required operations.

[87] The invention can also be embodied as computer readable code on a computer readable medium. The computer readable medium is any data storage device that can store data which can thereafter be read by a computer system. Examples of the computer readable medium include hard drives, network attached storage (NAS), read-only memory, random-access memory, CD-ROMs, CD-Rs, CD-RWs, magnetic tapes, and other optical and non-optical data storage devices. The computer readable medium can also be distributed over a network coupled computer systems so that the computer readable code is stored and executed in a distributed fashion.

[88] It will be further appreciated that the instructions represented by the operations in any of the above figures are not required to be performed in the order illustrated, and that all the processing represented by the operations may not be necessary to practice the invention. Further, the processes described in any of the above figures can also be implemented in software stored in any one of or combinations of the RAM, the ROM, or the hard disk drive.

[89] Although the foregoing invention has been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope and equivalents of the appended claims.

What is claimed is:

Claims

1. A method of processing a substrate comprising:

loading a substrate into a plasma chamber;

setting a pressure of the plasma chamber to a pre-determined pressure set point;

heating a plurality of inner surfaces defining a plasma zone to a processing temperature greater than about 200 degrees C;

injecting a process gas into the plasma zone to form a plasma; and

processing the substrate.

2. The method of claim 1, further comprising drawing a byproduct vapor from the plasma zone through a cold trap to condense the byproduct vapor in the cold trap.

3. The method of claim 2, wherein the cold trap has a temperature of not less than about 50 degrees C cooler than the processing temperature.

4. The method of claim 1, wherein processing the substrate includes etching the substrate.

5. The method of claim 1, wherein processing the substrate includes etching a copper film on the substrate

6. The method of claim 1, wherein heating the plurality of inner surfaces defining the plasma zone to the processing temperature includes maintaining a surface of the substrate at a second temperature sufficient to cause a byproduct vapor to condense on the surface of the substrate to deposit a film on the substrate.

7. The method of claim 6, wherein the second temperature is not less than about 50 degrees C cooler than the processing temperature.

8. The method of claim 1, wherein the pre-determined pressure set point is less than atmospheric pressure.

9. The method of claim 1, wherein the pre-determined pressure set point is within a range of about 1 mTorr and about 500 mTorr.

10. The method of claim 1, wherein the plasma chamber is a small volume plasma chamber.

11. The method of claim 10, wherein the small volume plasma chamber includes:

a first electrode, the first electrode forming a chuck for supporting the substrate; and

a second electrode, the second electrode being deposed substantially parallel to the first electrode, the second electrode being one of the plurality of inner surfaces, the first electrode and second electrode being separated by a predetermined distance.

12. The method of claim 11, wherein the predetermined distance is equal to a range of between about 0.5 cm and about 5 cm.

13. The method of claim 10, wherein the small volume plasma chamber includes a hot liner, wherein the hot liner forms a portion of the plurality of inner surfaces.

14. The method of claim 1, wherein processing the substrate includes a stress free planarization.

15. The method of claim 14, wherein the substrate is patterned, having a conductive interconnect material filling a plurality of features in the pattern, the conductive interconnect material having an overburden portion having at least one non-uniformity and wherein the stress free planarization includes:

planarizing the overburden portion including:

depositing an additional layer on the overburden portion; and

planarizing the additional layer and the overburden portion, the additional layer being substantially entirely removed in the planarizing process.

16. A small volume plasma chamber comprising:

a first electrode, the first electrode forming a chuck for supporting the substrate;

a second electrode, the second electrode being deposed substantially parallel to the first electrode, the first electrode and second electrode being separated by a predetermined distance; and

a hot liner, wherein the hot liner and the second electrode form a portion of a plurality of inner surfaces to define a plasma zone.

17. The small volume plasma chamber of claim 16, wherein the predetermined distance is equal to a range of between about 0.5 cm and about 5 cm.

18. The small volume plasma chamber of claim 16, further comprising a cold trap, the cold trap being sufficiently cooler than the plurality of inner surfaces that define the plasma zone to substantially cause a plasma byproduct vapor to condense in the cold trap, the cold trap being coupled to the plasma zone by a passage.

19. A semiconductor device formed by a method comprising:

loading a patterned substrate into a plasma chamber, the substrate having a conductive interconnect material filling a plurality of features in the pattern, the conductive interconnect material having an overburden portion having at least one non-uniformity;

setting a pressure of the plasma chamber to a pre-determined pressure set point;

heating a plurality of inner surfaces defining a plasma zone to a processing temperature of greater than about 200 degrees C;

injecting a process gas into the plasma zone to form a plasma;

processing the substrate including:

forming an additional layer on the overburden portion; and

planarizing the additional layer and the overburden portion, the additional layer being substantially entirely removed in the planarizing process; and

drawing a byproduct vapor from the plasma zone through a cold trap to condense the byproduct vapor in the cold trap.

20. The method of claim 19, wherein the conductive interconnect material includes copper.