## Claims

1. Process for the production of a layer structure of a nitride semiconductor component on a silicon surface, including the steps:
   - provision of a substrate that has a silicon surface;
   - deposition of an aluminium-containing nitride nucleation layer on the silicon surface of the substrate;
   - optional: deposition of an aluminium-containing nitride buffer layer on the nitride nucleation layer;
   - deposition of a masking layer on the nitride nucleation layer or, where present, on the first nitride buffer layer;
   - deposition of a gallium-containing first nitride semiconductor layer on the masking layer,

   wherein the masking layer is deposited in such a way that, in the deposition step of the first nitride semiconductor layer, initially separate crystallites grow that coalesce above a coalescence layer thickness and occupy an average surface area of ~~at least~~ between 0.16 $\mu m^2$ and 0.36 $\mu m^2$ per crystallite in a layer plane of the coalesced nitride semiconductor layer that is perpendicular to the growth direction,
   the masking layer is deposited in a layer thickness that permits that the first nitride semiconductor layer initially growing in the form of growth islands can, from a distance of on average at least 600 nm from the masking layer, form a layer area that is at least 80% closed,
   and
   the masking layer is deposited with a coverage of underlying nitride nucleation layer, or if present, of the first nitride buffer layer, of at least 95%.

~~2. Process according to claim 1, in which the masking layer is deposited in a layer thickness that in the first nitride semiconductor layer, which initially grows in the form of growth islands, leads to a layer area that is at least 80% closed from a distance of, on average, at least 600 nm from the masking layer.~~

~~3. Process according to claim 1 or 2, in which the masking layer is deposited with a coverage of the underlying nitride nucleation layer or, if present, of the first nitride buffer layer, of at least 95%.~~

42. Process according to ~~one of claims~~ Claim 1 ~~to 3,~~ in which the masking layer consisting of silicon nitride is deposited ~~from silicon nitride~~.

~~5~~3. Process according to ~~one of the preceding claims~~ Claim 1 or 2, in which the duration of the deposition of the masking layer is chosen so that in the deposition step of the first nitride semiconductor layer a concomitant measurement of the reflection intensity of the growth surface at a light wavelength of ca. 600 nm shows an oscillating intensity behaviour with increasing oscillation amplitude, which after at least 5 oscillation cycles reaches a maximum value that then remains ~~roughly~~ constant.

~~6~~4. Process according to one of ~~the preceding claims~~ Claims 1 to 3, in which the deposition of the nitride nucleation layer takes place on a (111) silicon surface.

~~7~~5. Process according to one of ~~the preceding claims~~ Claims 1 to 4, in which the first nitride semiconductor layer is deposited in a layer thickness of between 800 nm and 1600 nm.

~~8~~6. Process according to ~~claim 7~~ Claim 5, in which an aluminium-containing nitride intermediate layer is deposited on the first nitride semiconductor layer and in which a gallium-containing, further~~, second~~ nitride semiconductor layer is deposited on the last layer.

~~9~~7. Process according to ~~claim 8~~ Claim 6, in which the sequence of steps of the deposition of ~~an~~ the aluminium-containing nitride intermediate layer and ~~a~~ the gallium-containing further nitride semiconductor layer ~~are~~ is carried out repeatedly.

~~10~~8. Process according to ~~claim~~ Claim ~~8~~ 6 or ~~9~~ 7, in which a multi-quantum-well structure consisting of nitride semiconductor material is deposited on the further nitride semiconductor layer.

~~11~~9. Process according to ~~claim 10~~ Claim 8, characterised by the deposition of at least one further masking layer consisting of silicon nitride immediately before the deposition of those of the further nitride semiconductor layers on which the multi-quantum-well structure is deposited.

~~12~~10. Process according to ~~one of the preceding claims~~ Claim 1 or 2, in which an n-doping is introduced into the first and, if present, those further nitride semiconductor layers that are deposited before the multi-quantum-well structure.

~~13~~11. Process according to ~~one of the preceding claims~~ Claim 1 or 2, comprising ~~the following steps:~~ a production of a p-doped, gallium-containing nitride semiconductor cover layer on the multi-quantum-well structure.

~~14~~12. Process according to ~~one of the preceding claims~~ Claim 1 or 2, in which the step of providing a substrate includes the provision of a silicon substrate, the thickness of which is at least ~~$D_{GaN} \times x$~~ $D_{GaN}{}^{*}x$, wherein $D_{GaN}$ denotes the layer thickness of the nitride semiconductor layer to be deposited on the substrate or, if more than one nitride semiconductor layer is to be deposited, denotes the sum of the layer thicknesses of the nitride semiconductor layers to be deposited on the substrate and of the existing nitride intermediate layer, and wherein x in the case where a doped silicon substrate is used is 110 and in the case where an undoped substrate is used is 200.

~~15~~13. Process according to ~~claim 14~~ Claim 12, in which the step of providing a substrate includes the provision of a silicon substrate, the thickness of which is additionally greater than or equal to ~~$100 \times \sqrt{D_{GaN}} \times y$,~~

$$100 * \sqrt{D_{GaN}} * y$$

where ~~$y = \frac{Substrate\ diameter\ in\ cm}{3.5}$~~ y = substrate diameter in cm / 3.5.

~~16~~14. Process for the production of a nitride semiconductor component, comprising the steps:

- production of a layer structure of a nitride semiconductor component on a silicon surface according to one of the preceding claims;
- bonding of the layer structure to a carrier in such a way that the growth upper side of the layer structure is facing the carrier;
- either complete or partial removal of the substrate;
- production of a contact structure.

~~17. Process according to claim 16, with a step involving the deposition of an electrically conducting contact layer on the growth upper side of the layer structure.~~

~~18. Process according to claim 17, in which for the contact layer a material is used that has a higher refractive index than the p-doped nitride semiconductor cover layer.~~

~~19. Process according to one of claims 16 to 18, with a step, carried out before the bonding, involving metallisation of the growth upper side of the layer structure or, if present, of the contact layer.~~

~~20. Process according to one of claims 16 to 19, in which a carrier is used whose surface that is employed for the bonding is electrically conducting or reflecting or metallic.~~

21. Process according to one of claims 18 to 20, in which the nitride semiconductor cover layer of the layer structure is deposited in a thickness of $m \cdot \frac{\lambda}{2 \cdot n_{nitride}} + \frac{\lambda}{4 \cdot n_{nitride}} - \frac{d_{MQW}}{2}$, where m = 0, 1, 2, 3, ...; $\lambda$ is a wavelength of a light emission of the multi-quantum-well structure during operation of the nitride semiconductor component, $n_{nitride}$ is the refractive index of the nitride at the wavelength $\lambda$, and $d_{MQW}$ denotes the thickness of the multi-quantum-well structure.

22. Process according to claim 17, in which a material is used for the contact layer that has a smaller refractive index than the p-doped nitride semiconductor cover layer.

23. Process according to claim 22, in which the nitride semiconductor cover layer of the layer structure is deposited in a thickness of $m \cdot \frac{\lambda}{2 \cdot n_{nitride}} - \frac{d_{MQW}}{2}$, where m = 1, 2, 3, 4, ...; $\lambda$ is a wavelength of a light emission of the multi-quantum-well structure in the operation of the nitride semiconductor component, $n_{nitride}$ denotes the refractive index of the nitride at the wavelength $\lambda$, and $d_{MQW}$ denotes the thickness of the multi-quantum-well structure.

24. Process according to one of claims 16 to 23, in which the bonding is carried out at a temperature in the range between 280 and 500°C.

25. Process according to one of claims 16 to 24, in which the step of removing the substrate is carried out by grinding or by combined grinding and etching.

~~26. Process according to one of claims 16 to 24, in which the step of removing the substrate is carried out solely by etching.~~

~~27. Process according to one of claims 16 to 25, in which the growth rear side exposed by the removal of the substrate is structured for the formation of an anti-reflection-acting layer.~~

~~28~~15. Nitride semiconductor component with

- a gallium-containing first nitride semiconductor layer that has a structure of coalesced crystallites that occupy an average surface area of ~~at least~~ between 0.16 $\mu m^2$ and 0.36 $\mu m^2$ per crystallite in a layer plane perpendicular to the growth direction,
- an aluminium-containing nitride intermediate layer that adjoins the first nitride semiconductor layer, and
- a gallium-containing further, second nitride semiconductor layer adjoining the last layer.

~~29~~16. Nitride semiconductor component according to ~~claim 28~~ Claim 15, in which the crystallites in a layer plane perpendicular to the growth direction have an average size of at least 400 x 400 $nm^2$.

~~30. Nitride semiconductor component according to claim 28, in which the crystallites in a layer plane perpendicular to the growth direction occupy an average surface area of at least 0.36 $\mu m^2$.~~

~~31~~17. Nitride semiconductor component according to ~~one of claims 28 to 30~~ Claim 15 or 16, in which the first nitride semiconductor layer has a layer thickness of between 800 nm and 1600 nm.

~~32~~18. Nitride semiconductor component according to one of ~~claims 28 to 31~~ Claims 15 to 17, that repeatedly contains the layer sequence of

aluminium-containing nitride intermediate layer and gallium-containing further nitride semiconductor layer.

~~33~~19. Nitride semiconductor component according to ~~one of claims 31 or 32~~ Claim 17 or 18, in which a multi-quantum-well structure consisting of nitride semiconductor material is deposited on the further nitride semiconductor layer.

~~34~~20. Nitride semiconductor component according to ~~claim 33~~ Claim 19, characterised by at least one further masking layer consisting of silicon nitride immediately adjoining ~~that layer of~~ the further nitride semiconductor layers on which the multi-quantum-well structure is deposited, but on the side of this further nitride semiconductor layer facing away from the multi-quantum-well structure.

~~35~~21. Nitride semiconductor component according to one of ~~claims 28 to 34~~ Claims 15 to 19, in which the first and, where present, those further nitride semiconductor layers that are arranged on the side of the multi-quantum-well structure that faces towards the first nitride semiconductor layer, are n-doped.

~~36~~22. Nitride semiconductor component according to one of ~~claims 33 to 35~~ Claims 15 to 21, with a p-doped, gallium-containing nitride semiconductor cover layer that is arranged on the side of the multi-quantum-well structure facing away from the first nitride semiconductor layer.

~~37~~23. Nitride semiconductor component according to one of ~~claims 28 to 36~~ Claims 15 to 22, with a carrier that is bonded to the first nitride semiconductor layer.

~~38. Nitride semiconductor component according to one of claims 28 to 37, in which the carrier and the first nitride semiconductor layer are bonded to one another via a metal layer.~~

~~39. Nitride semiconductor component according to claim 37 or 38, in which the carrier consists primarily of copper or aluminium or silicon or aluminium nitride or of Al/Si.~~

4024. Nitride semiconductor component according to one of ~~claims 28 to 39~~ Claims 15 to 23, in which an electrically conducting contact layer is arranged between the carrier and the first nitride semiconductor layer.

~~41. Nitride semiconductor component according to claim 36 and claim 40, in which the contact layer has a higher refractive index than the p-doped nitride semiconductor cover layer.~~

4225. Nitride semiconductor component according to ~~claim 36~~ Claim 22, in which the nitride semiconductor cover layer of the layer structure is deposited in a thickness of ~~$m \cdot \frac{\lambda}{2 \cdot n_{nitride}} + \frac{\lambda}{4 \cdot n_{nitride}} - \frac{d_{MQW}}{2}$~~,

$$m \cdot \frac{\lambda}{2 \cdot n_{\underline{Nitride}}} + \frac{\lambda}{4 \cdot n_{\underline{Nitride}}} - \frac{d_{MQW}}{2}$$

where m = 0, 1, 2, 3, ...; $\lambda$ is a wavelength of a light emission of the multi-quantum-well structure during operation of the nitride semiconductor component, ~~$n_{nitride}$~~ $n_{\underline{Nitride}}$ is the refractive index of the nitride at the wavelength $\lambda$, and $d_{MQW}$ denotes the thickness of the multi-quantum-well structure.

~~43. Nitride semiconductor component according to claim 36 and claim 40, in which the contact layer has a lower refractive index than the p-doped nitride semiconductor cover layer.~~

4426. Nitride semiconductor component according to ~~claim 43~~ Claim 24, in which the nitride semiconductor cover layer of the layer structure ~~is deposited in~~ has a thickness of ~~$m \cdot \frac{\lambda}{2 \cdot n_{nitride}} - \frac{d_{MQW}}{2}$~~,

$$m \cdot \frac{\lambda}{2 \cdot n_{Nitride}} - \frac{d_{MQW}}{2}$$

where m = 1, 2, 3, 4, ...; $\lambda$ is a wavelength of a light emission of the multi-quantum-well structure during operation of the nitride semiconductor component, ~~$n_{nitride}$~~ $n_{Nitride}$ is the refractive index of the nitride at the wavelength $\lambda$, and $d_{MQW}$ denotes the thickness of the multi-quantum-well structure.

~~45. Nitride semiconductor component according to one of claims 28 to 44, with an n-side and a p-side electrical contact element.~~

4627. Carrier wafer with a plurality of nitride semiconductor components according to one of ~~claims 28 to 45~~ Claims 15 to 26.

4728. Carrier wafer according to ~~claim 46~~ Claim 27, in which the plurality of nitride semiconductor components on the carrier have in totality a lateral dimension of at least 24 cm.

4829. Nitride semiconductor product with

- a substrate that has a silicon surface,
- an aluminium-containing nitride nucleation layer adjoining the silicon surface,
- optional: an aluminium-containing nitride buffer layer adjoining the nitride nucleation layer,
- a masking layer on the nitride nucleation layer or, if present, on the nitride buffer layer, and with

– a gallium-containing first nitride semiconductor layer arranged adjoining the masking layer and having a structure of coalesced crystallites, in which the crystallites above a coalescence layer thickness and in a layer plane perpendicular to the growth direction occupy an average surface area ~~of at least~~ between 0.16 $\mu m^2$ and 0.36 $\mu m^2$ per crystallite.

~~49~~30. Nitride semiconductor product according to ~~claim 48~~ Claim 29, ~~in which~~ wherein the growth islands have coalesced in an amount of at least 80% at a distance of at least 600 nm from the masking layer.

~~50~~31. Nitride semiconductor product according to one of ~~claims 48 and 49~~ Claims 29 and 30, in which the nitride nucleation layer is an aluminium nitride layer or an aluminium/gallium nitride layer with an aluminium proportion of at least 10%.

~~51~~32. Nitride semiconductor product according to ~~claim 50~~ Claim 31, in which the nitride nucleation layer has a layer thickness of between 10 and ~~100~~ 50 nm.

~~52~~33. Nitride semiconductor product according to one of ~~claims 48 to 51~~ Claims 29 to 32, in which the nitride buffer layer has a layer thickness of at most 400 nm.

~~53~~34. Nitride semiconductor product according to one of ~~claims 48 to 52~~ Claims 29 to 33, in which the substrate in a direction perpendicular to ~~the~~ a rear side substrate surface is either free of curvature or has a radius of curvature of at least 10 m.

~~54~~35. Nitride semiconductor product according to one of ~~claims 48 to 53~~ Claims 29 to 34, with an aluminium-containing nitride intermediate layer that adjoins the first nitride semiconductor layer and,

——with a gallium-containing further, second nitride semiconductor layer adjoining the last layer.

~~55. Nitride semiconductor product according to one of claims 48 to 54, in which the crystallites in a layer plane perpendicular to the growth direction occupy an average surface area of at least 0.36 $\mu m^2$.~~

~~56~~36. Nitride semiconductor product according to one of ~~claims 48 to 55~~ Claims 29 to 35, in which the substrate has a lateral dimension of at least 24 cm.