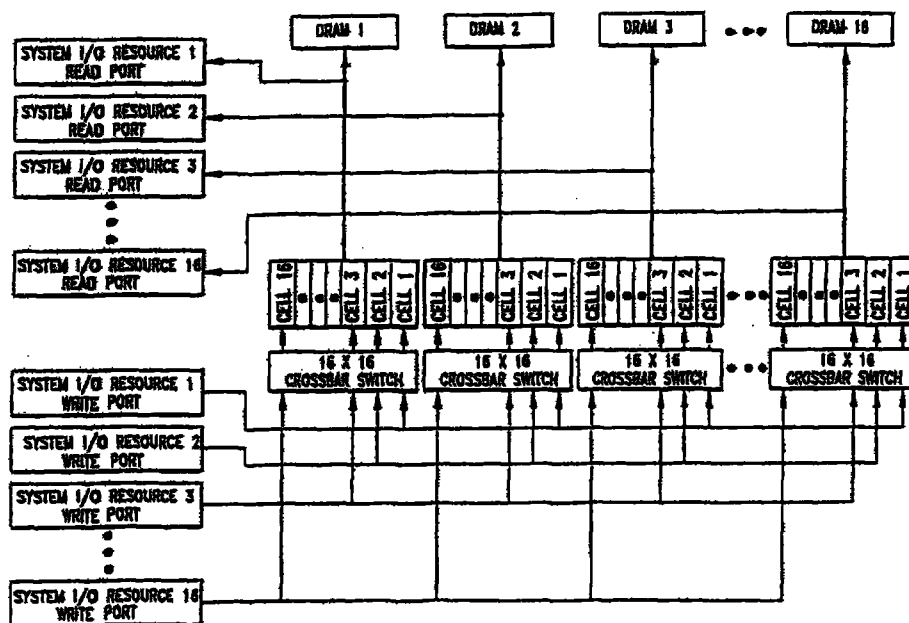




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(54) Title: AMPIC DRAM SYSTEM IN A TELECOMMUNICATION SWITCH



(57) Abstract

A technique and system for eliminating bus contention in multi-port internally cached dynamic random access memory (AMPIC DRAM) systems, while eliminating the need for external control paths and random memory addressing, through the use of data header destination bits and a novel dedication of reduced size slot buffers to separate DRAM banks and similarly dedicated I/O data read resource ports, particularly useful for relatively short ATM message networking and the like, wherein all system I/O resources are enabled simultaneously to write complete ATM messages into a single slot buffer, and also for SONET Cross Connect and WDM messages.