FIG. 1

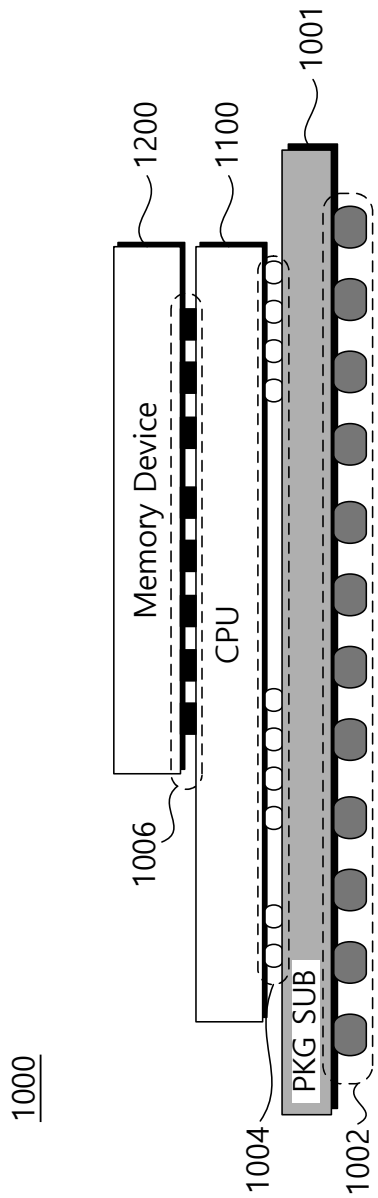


FIG. 2

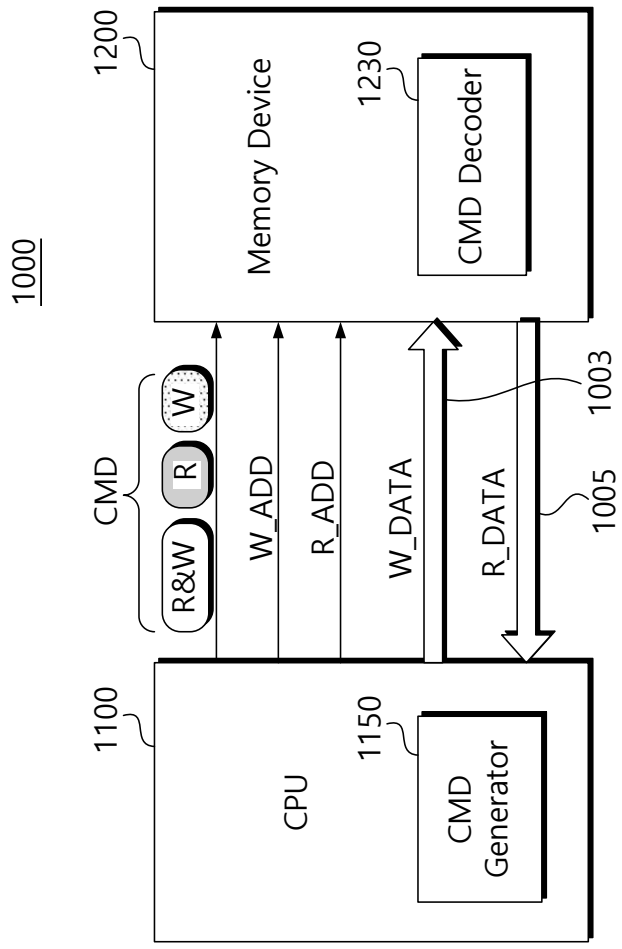

1000
1200
Memory Device
1230
CMD Decoder
CMD
R&W
R
W
W_ADD
R_ADD
W_DATA
R_DATA
1003
1005
1100
CPU
1150
CMD Generator

FIG. 3

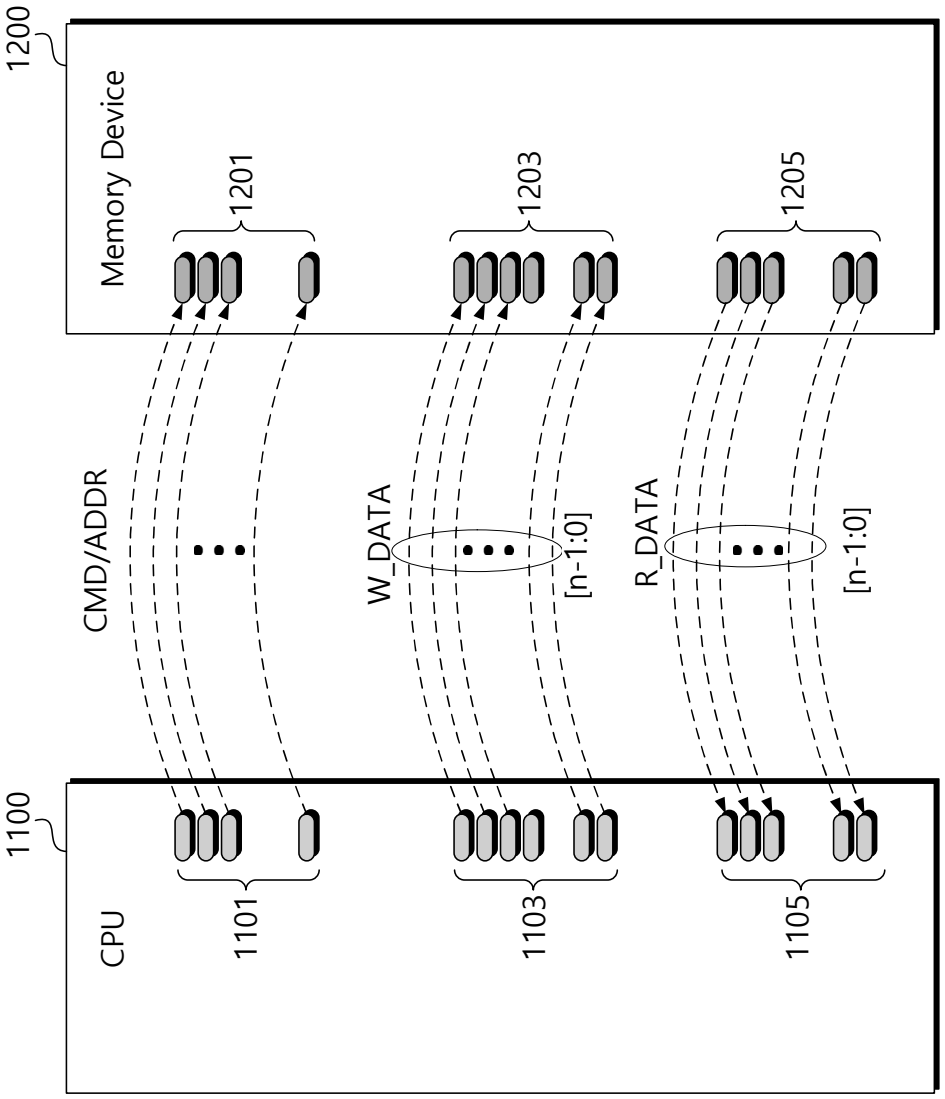

1200
Memory Device
1201
1203
1205
CMD/ADDR
W_DATA
[n-1:0]
R_DATA
[n-1:0]
1100
CPU
1101
1103
1105

FIG. 4

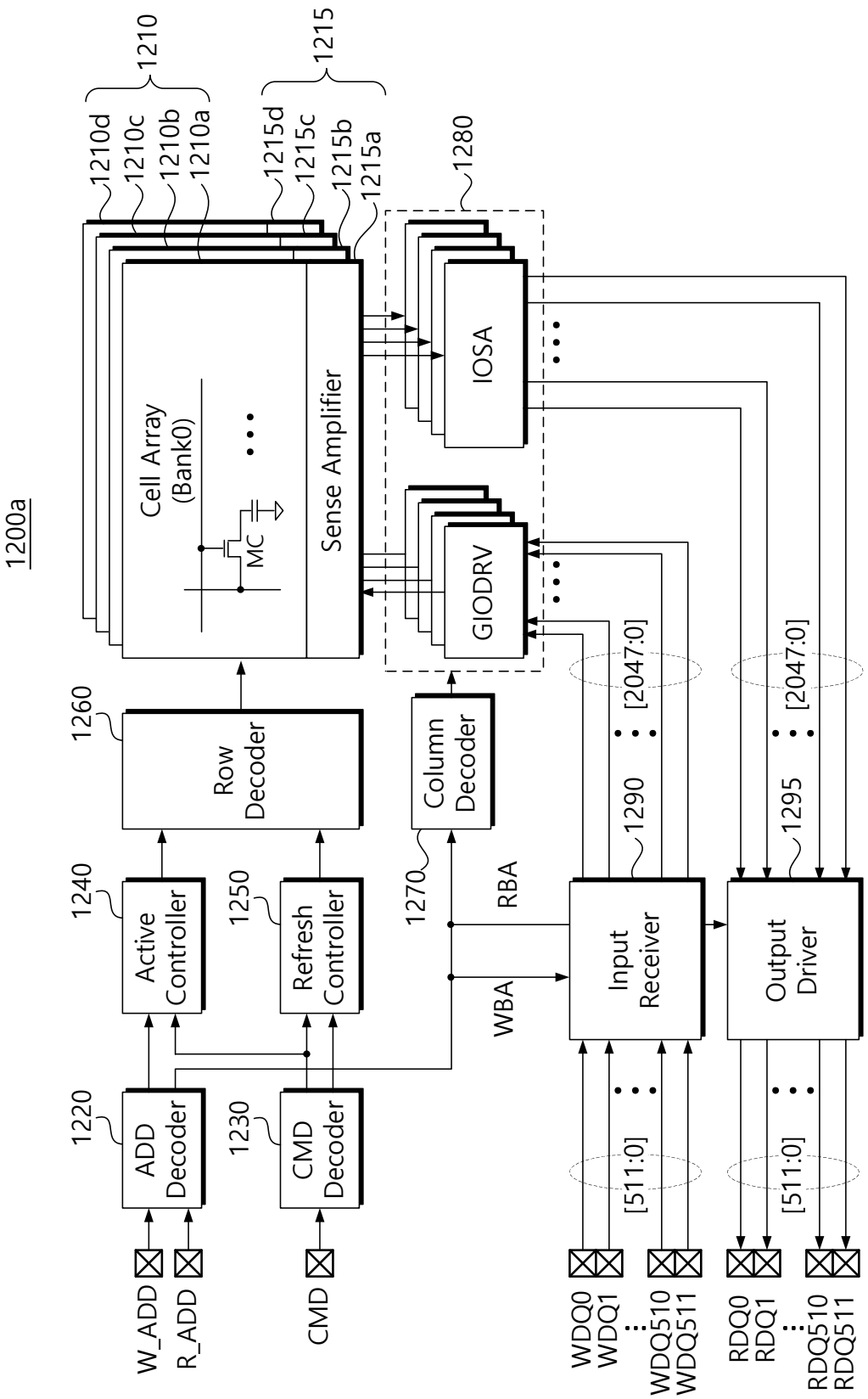

1200a
1210
1215
1210d
1210c
1210b
1210a
1215d
1215c
1215b
1215a
1280
Cell Array
(Bank0)
MC
Sense Amplifier
IOSA
GIODRV
1260
Row
Decoder
Column
Decoder
1240
Active
Controller
1250
Refresh
Controller
1270
RBA
WBA
1290
1295
[2047:0]
[2047:0]
Input
Receiver
Output
Driver
1220
ADD
Decoder
1230
CMD
Decoder
[511:0]
[511:0]
W_ADD
R_ADD
CMD
WDQ0
WDQ1
WDQ510
WDQ511
RDQ0
RDQ1
RDQ510
RDQ511

FIG. 5

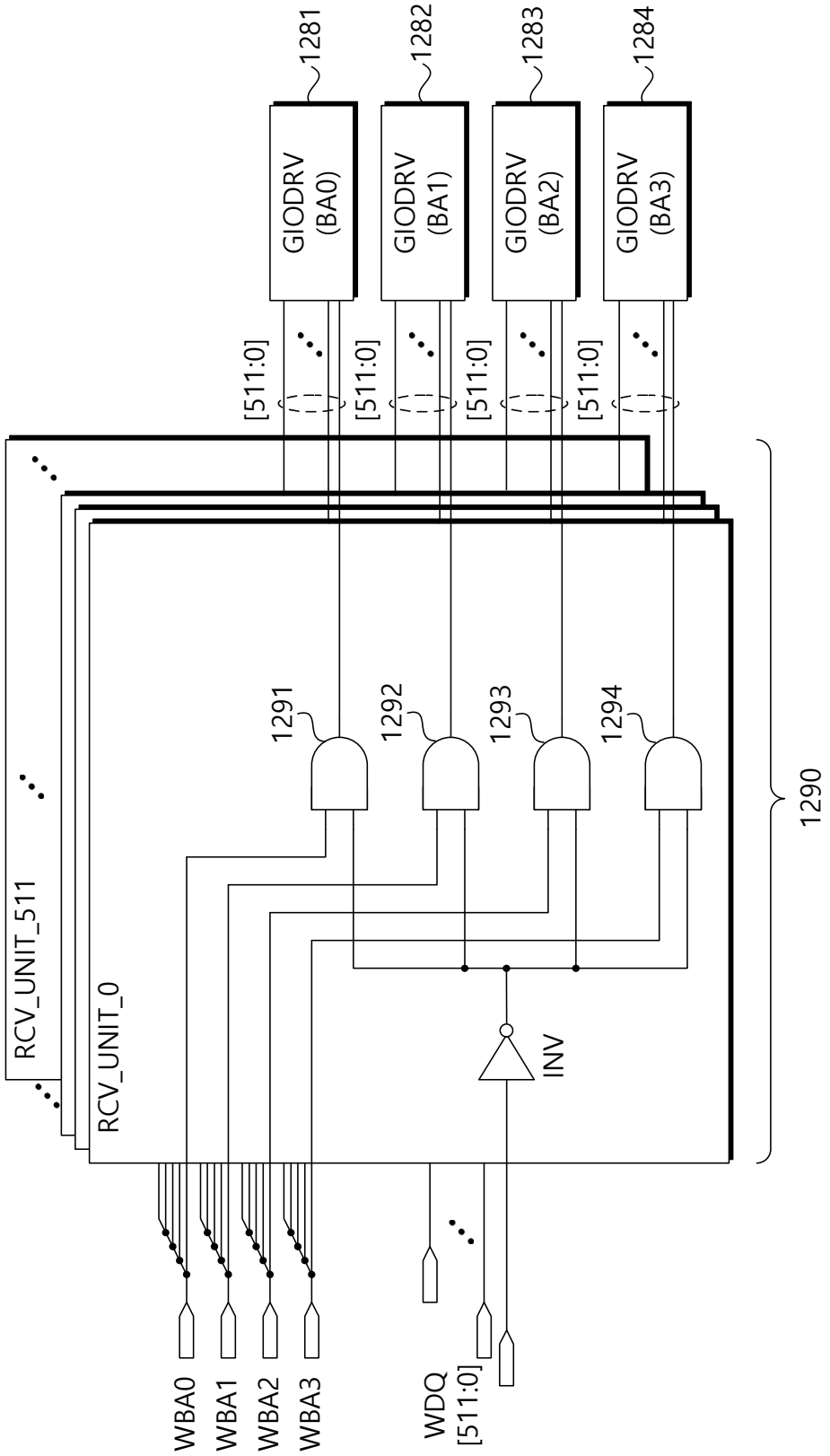

1281
1282
1283
1284
GIODRV (BA0)
GIODRV (BA1)
GIODRV (BA2)
GIODRV (BA3)
[511:0]
[511:0]
[511:0]
[511:0]
RCV_UNIT_511
RCV_UNIT_0
1291
1292
1293
1294
INV
1290
WBA0
WBA1
WBA2
WBA3
WDQ [511:0]

FIG. 6

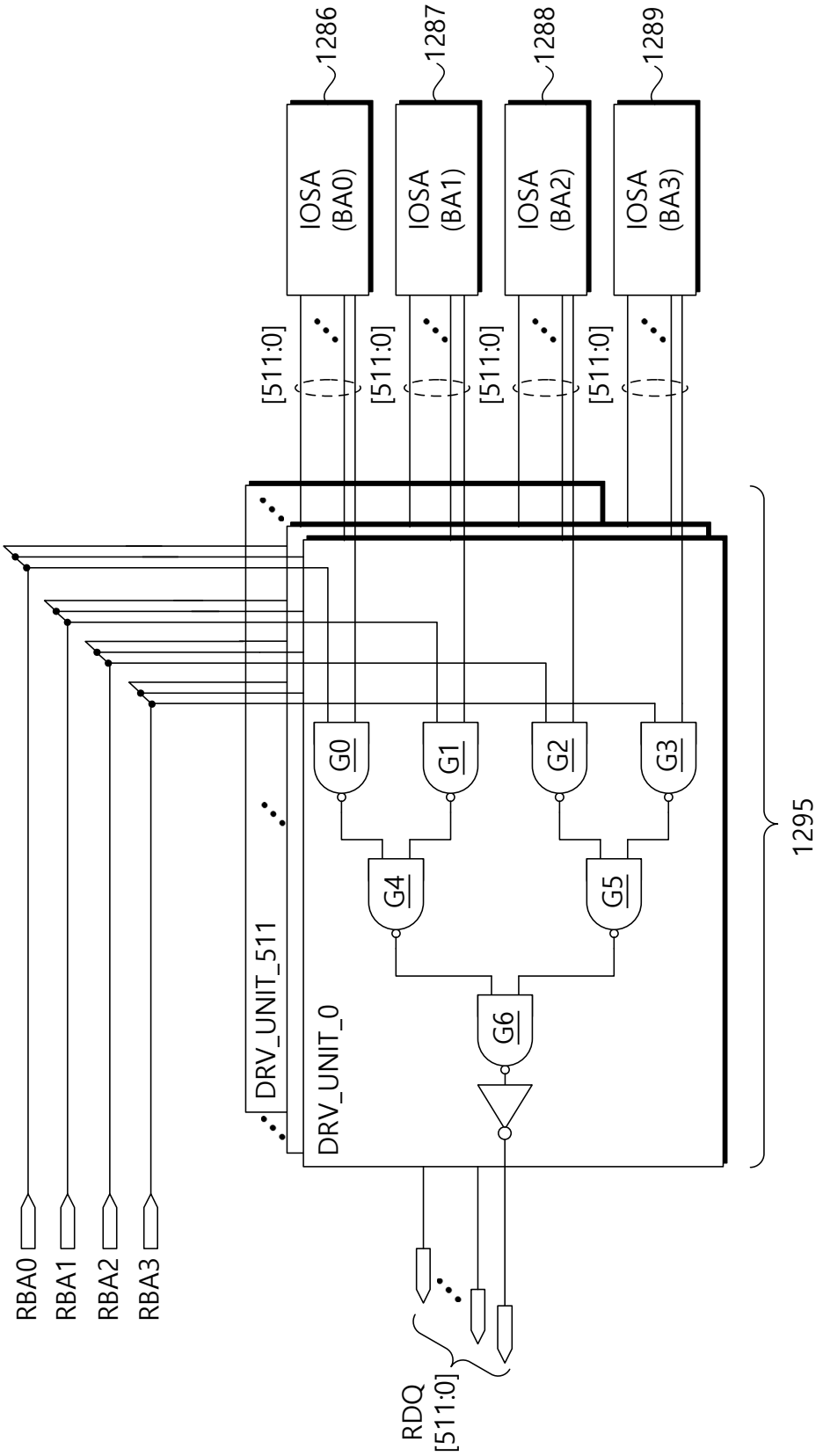

1286
1287
1288
1289
IOSA (BA0)
IOSA (BA1)
IOSA (BA2)
IOSA (BA3)
[511:0]
[511:0]
[511:0]
[511:0]
G0
G1
G2
G3
G4
G5
G6
DRV_UNIT_511
DRV_UNIT_0
1295
RBA0
RBA1
RBA2
RBA3
RDQ [511:0]

FIG. 7

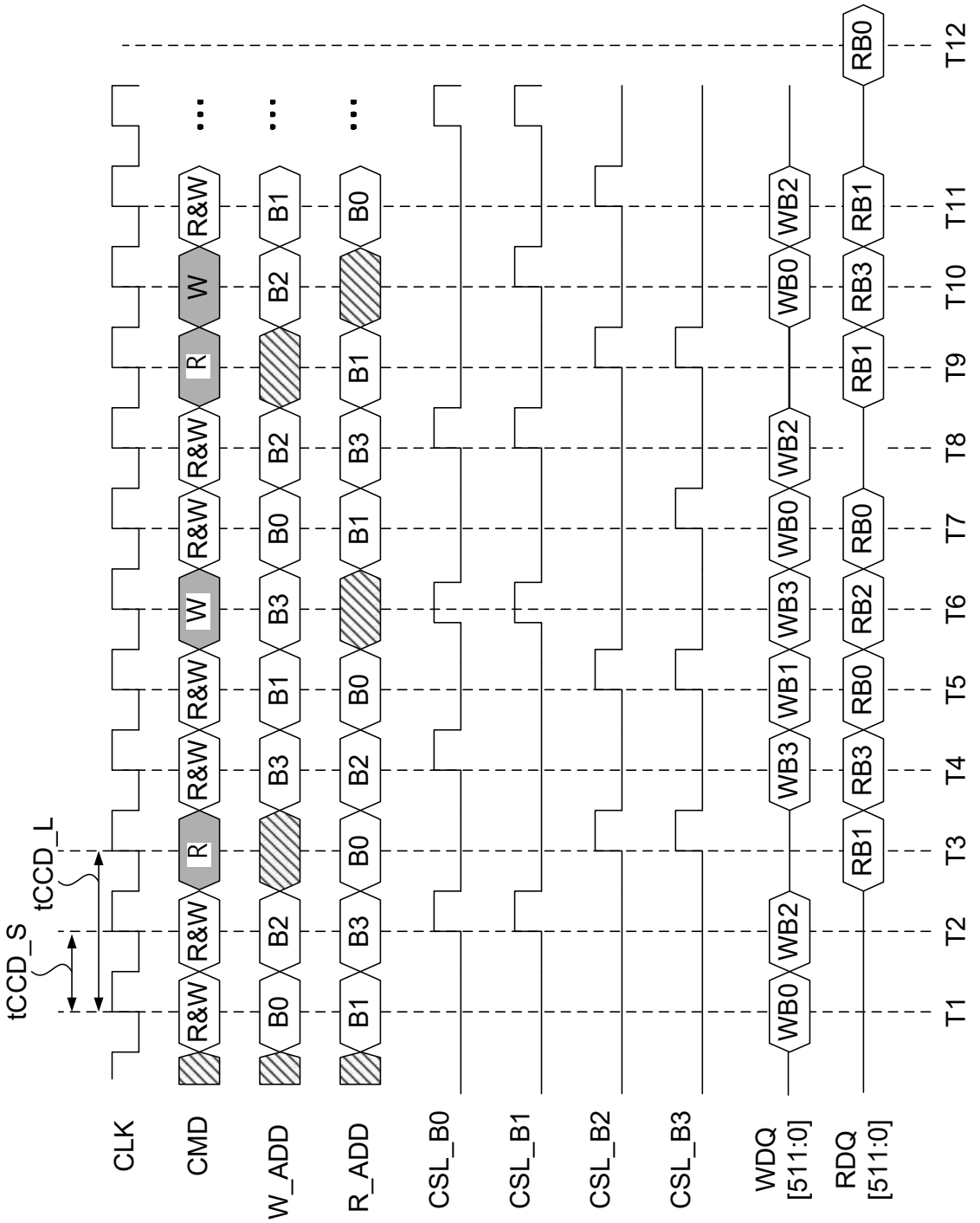

tCCD_S
tCCD_L
CLK
CMD
W_ADD
R_ADD
CSL_B0
CSL_B1
CSL_B2
CSL_B3
WDQ [511:0]
RDQ [511:0]
R&W
R
W
B0
B1
B2
B3
WB0
WB1
WB2
WB3
RB0
RB1
RB2
RB3
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12

FIG. 8

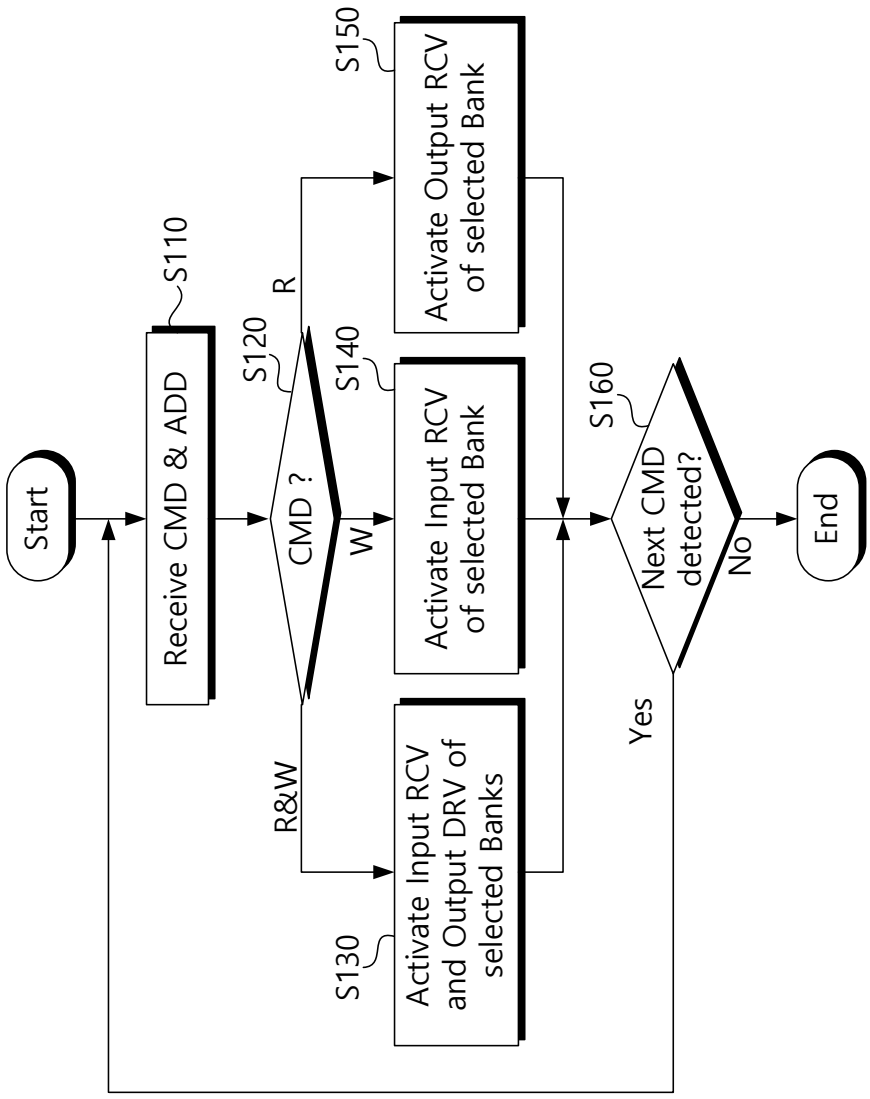

Start
Receive CMD & ADD
S110
CMD ?
S120
R
W
R&W
Activate Output RCV of selected Bank
S150
Activate Input RCV of selected Bank
S140
Activate Input RCV and Output DRV of selected Banks
S130
Next CMD detected?
S160
Yes
No
End

FIG. 9

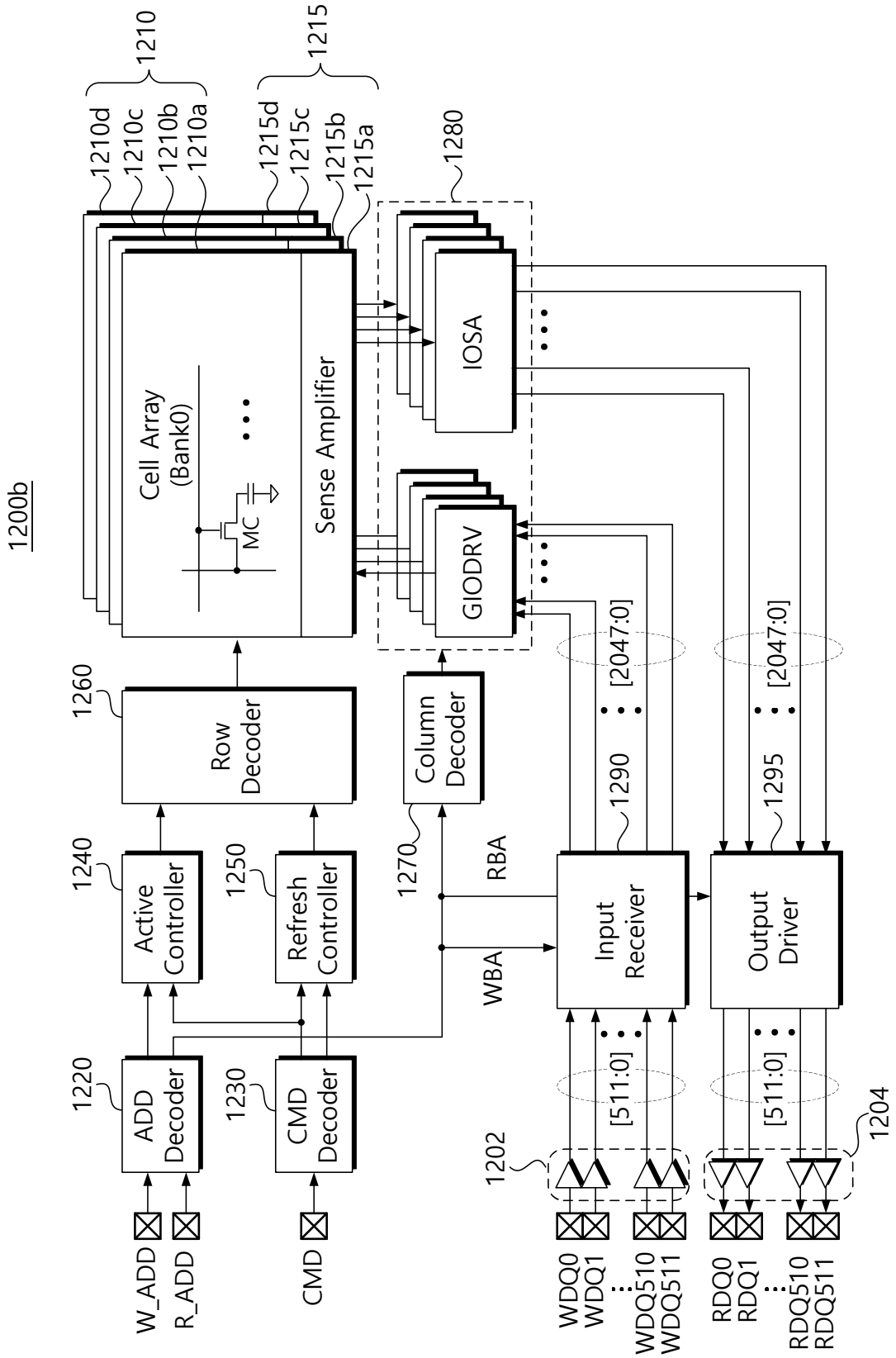

1200b
1210
1215
1210d
1210c
1210b
1210a
1215d
1215c
1215b
1215a
1280
Cell Array
(Bank0)
MC
Sense Amplifier
IOSA
GIODRV
1260
Row
Decoder
Column
Decoder
1240
Active
Controller
1250
Refresh
Controller
1270
RBA
WBA
1290
1295
[2047:0]
[2047:0]
Input
Receiver
Output
Driver
1220
ADD
Decoder
1230
CMD
Decoder
[511:0]
[511:0]
1202
1204
W_ADD
R_ADD
CMD
WDQ0
WDQ1
WDQ510
WDQ511
RDQ0
RDQ1
RDQ510
RDQ511

FIG. 10

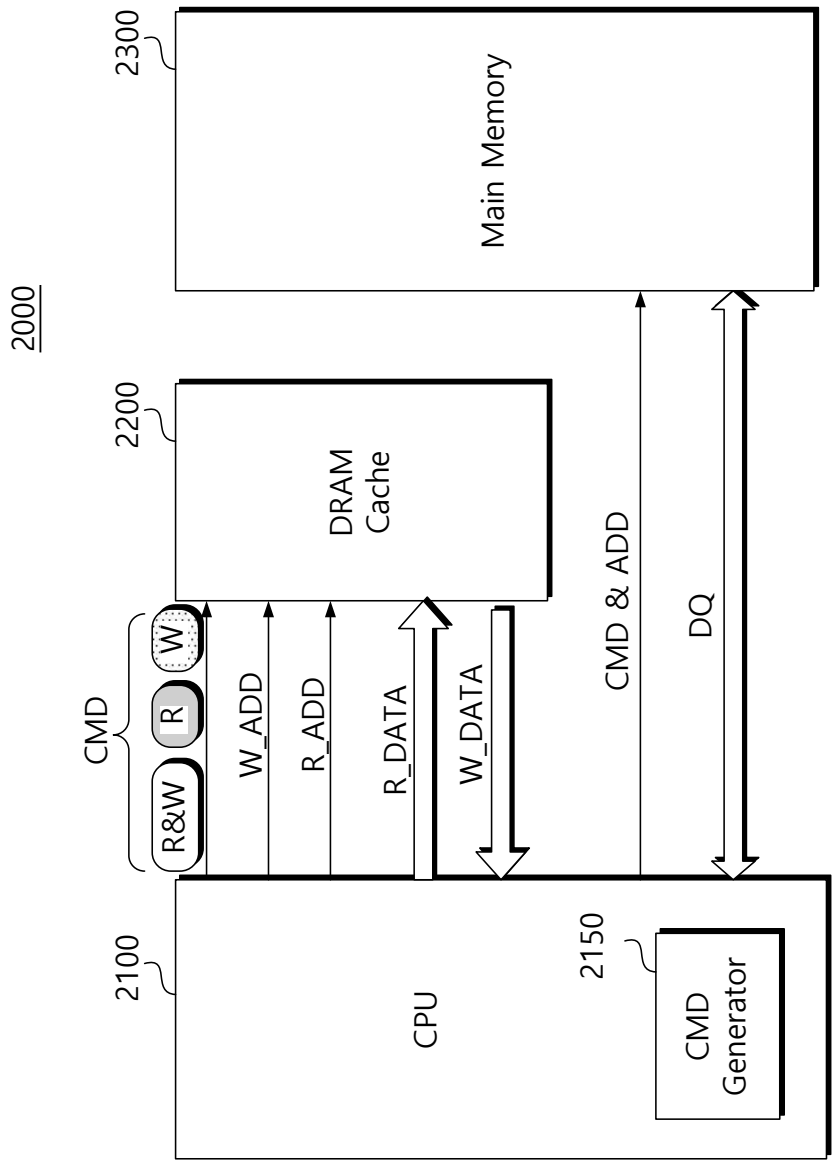
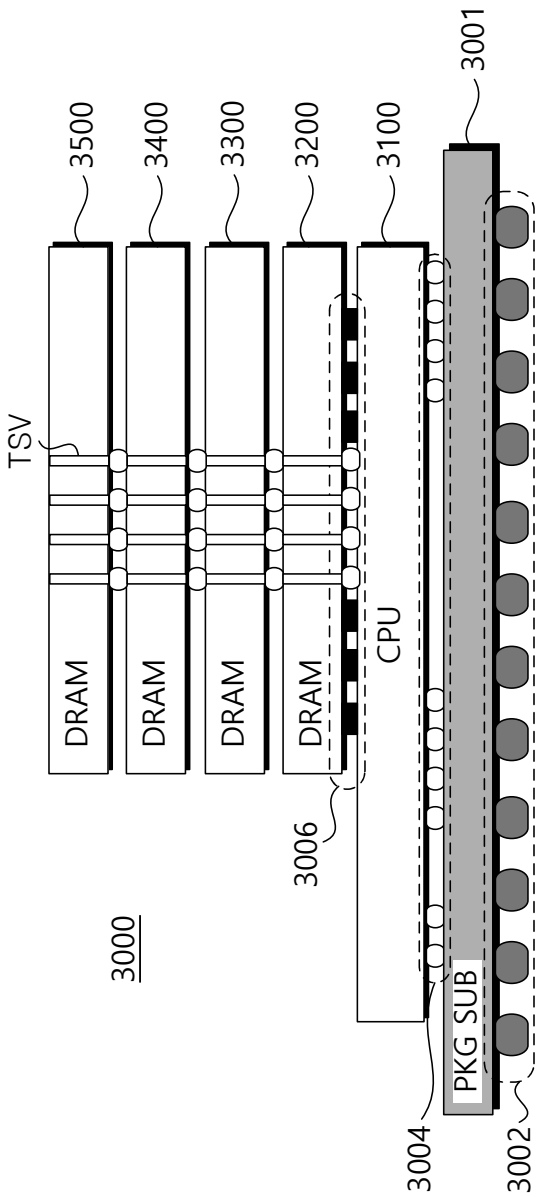

2000
2300
Main Memory
2200
DRAM Cache
CMD
R&W
R
W
W_ADD
R_ADD
R_DATA
W_DATA
CMD & ADD
DQ
2100
CPU
2150
CMD Generator

FIG. 11


3000
3500
3400
3300
3200
3100
3001
TSV
DRAM
DRAM
DRAM
DRAM
CPU
3006
PKG SUB
3004
3002