

STRUCTURE AND MATERIAL ENGINEERING METHODS FOR OPTOELECTRONIC DEVICES SIGNAL TO NOISE RATIO ENHANCEMENT

FIELD

[0001] Embodiments described herein are generally related to an optoelectronic device, and more specifically, an image sensor that has an epitaxially grown charge layer on surfaces of pixels to enhance signal-to-noise ratio in the image sensor.

BACKGROUND

[0002] Complementary metal-oxide-semiconductor (CMOS) image sensors (CIS) are widely used in various applications such as digital cameras and mobile phones. A CIS uses an array of pixels, such as photodiodes, photogate detectors, or phototransistors, for collecting light projected towards a semiconductor substrate and converting collected photo-energy into electrical signals that can be used in a suitable application. One type of CIS, backside-illuminated (BSI) CIS, typically has a silicon substrate that includes an array of pixels formed inside for sensing and recording an intensity of light entering the substrate from the backside, and some circuitry and input/outputs adjacent the array of pixels for providing an operation environment for the pixels and for supporting external communication with the pixels. During device processing such as etching, polishing, or any other material removing process, a surface of the backside of the substrate (and thus surfaces of the pixels) is damaged and left with dangling bonds and/or defect centers. Charge carriers generated from such dangling bonds and/or defect centers contribute to the formation of noise in the electrical signals in the array of pixels.

[0003] Conventional methods for suppressing the generation of noise include passivating the surface of the backside of the substrate, by adding a charge layer (*i.e.*, a layer including charge carriers) near the surface of the backside of the substrate. Charge carriers in the charge layer recombine with charge carriers generated from the dangling bonds and/or defect centers. A charge layer may be formed by implanting a desired type of charges (*i.e.*, positive charges or negative charges that are opposite of the charge carriers generated from the dangling bonds and/or defect centers) into the substrate. Alternatively, a charge layer may be formed by adding a dielectric material on the surface of the backside of the substrate having the opposite type of

the desired type of charges, such that the desired type of charges is induced in the substrate near the backside. A buffer oxide layer may be inserted between the surface of the backside of the substrate and the dielectric material for charge separation between the charge carriers in the dielectric layer and the induced charge carriers in the substrate near the surface.

[0004] However, recent demand for deeper pixels with high aspect ratio trench isolation (*i.e.*, pixels separated from each other by high aspect ratio trenches) and higher signal-to-noise ratio brings challenges to the conventional methods. A charge layer formed by the conventional methods may not provide enough charge carriers to passivate the surface of the substrate with reasonable fabrication cost and design requirements. Furthermore, a charge layer formed by implantation may also not have a good coverage on sidewalls of trenches of high aspect ratio. A charge layer formed by a thick dielectric layer for better passivation of the induced charge carriers may also have a high absorption coefficient, leading to reduced signal from the array of pixels.

[0005] Therefore, there is a need in the art for an improved method for passivating a damaged surface of the backside of a BSI CIS device as well as any damaged surface from etch and/or polishing and more generally an improved structure of a BSI CIS device. The method can also be implemented on frontside-illuminated (FSI) CIS to provide similar benefits as for BSI CIS.

SUMMARY

[0006] In one embodiment, a method of fabricating a semiconductor device includes forming an interconnect structure over a front side of a sensor substrate, thinning the sensor substrate from a back side of the sensor substrate, etching trenches into the sensor substrate, pre-cleaning an exposed surface of the sensor substrate, epitaxially growing a charge layer directly on the pre-cleaned exposed surface of the sensor substrate, and forming isolation structures within the etched trenches.

[0007] In another embodiment, a method of fabricating a semiconductor device includes epitaxially growing a epitaxially grown layer directly on a surface of a handle substrate, epitaxially growing a semiconductor layer directly on the charge layer, implanting a dopant into the semiconductor layer, etching trenches into the semiconductor layer, forming isolation structures within the etched trenches, forming

an interconnect structure over the semiconductor layer, and removing the handle substrate from the epitaxially grown layer.

[0008] In yet another embodiment, an image sensor includes a sensor substrate having a front side and a back side, a plurality of pixels formed within the sensor substrate on the back side, a plurality of isolation structures formed within the sensor substrate, wherein the plurality of pixels are isolated from each other by one of the plurality of isolation structures, an interconnect structure over the front side of the sensor substrate, and a charge layer epitaxially grown directly on surfaces of the plurality of pixels on the back side of the sensor substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Implementations of the present disclosure, briefly summarized above and discussed in greater detail below, can be understood by reference to the illustrative implementations of the disclosure depicted in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical implementations of this disclosure and are therefore not to be considered limiting of its scope, for the disclosure may admit to other equally effective implementations.

[0010] FIG. 1 is a cross sectional view of a back-side illuminated (BSI) image sensor device fabricated according to a first embodiment of the present disclosure.

[0011] FIG. 2 is a cross sectional view of a back-side illuminated (BSI) image sensor device fabricated according to a second embodiment of the present disclosure.

[0012] FIG. 3 is a flowchart of a method for fabricating an image sensor device, such as a back-side illuminated (BSI) image sensor according to the first embodiment of the present disclosure.

[0013] FIGs. 4A, 4B, 4C, 4D, and 4E schematically illustrate intermediate steps performed in a method of fabricating an image sensor device, such as a back-side illuminated (BSI) image sensor according to the first embodiment of the present disclosure.

[0014] FIG. 5 is a flowchart of a method for fabricating an image sensor device, such as a back-side illuminated (BSI) image sensor device according to the second embodiment of the present disclosure.

[0015] FIGs. 6A, 6B, 6C, 6D, 6E, and 6F schematically illustrate intermediate steps performed in a method fabricating an image sensor device, such as a back-side illuminated (BSI) image sensor according to the second embodiment of the present disclosure.

[0016] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. The figures are not drawn to scale and may be simplified for clarity. It is contemplated that elements and features of one implementation may be beneficially incorporated in other implementations without further recitation.

DETAILED DESCRIPTION

[0017] Embodiments described herein are generally related to an optoelectronic device, and more specifically, an image sensor that has an epitaxially grown charge layer on surface of pixels to enhance signal to noise ratio in the image sensor.

[0018] Image sensors described herein include an epitaxially grown charge layer on a sensor substrate in which pixels are formed. Epitaxially grown charge layers conformally cover damaged surfaces of pixels where undesired carriers (noise) are generated from dangling bonds and/or defect centers caused by device fabrication processes. Epitaxially grown charge layers passivate the charge carriers at the surfaces of pixels, and thus are prevented from causing noise in the electrical signals converted from photo-energy in the pixels.

[0019] FIG. 1 is a cross sectional view of a back-side illuminated (BSI) image sensor device 100 fabricated according to a first embodiment of the present disclosure. The image sensor device 100 may be a charge coupled device (CCD), complementary metal oxide semiconductor (CMOS) image sensor (CIS), an active-pixel sensor (APS), or a passive-pixel sensor.

[0020] The image sensor device 100 includes a sensor substrate 102 having a front side 104 and a back side 106. The sensor substrate 102 may be a photodiode. In some embodiments, the sensor substrate 102 includes a pinned layer photodiode, a photogate, a reset transistors, a source follower transistor, or a transfer transistor. The sensor substrate 102 is operable to sense incident light 110 that is projected toward the back side 106 of the sensor substrate 102. The sensor substrate 102 absorbs

photo-energy of the projected incident light 110 and creates electron-hole pairs near the back side 106 of the sensor substrate 102, inducing mobile charge carriers. The charge carriers are diffused and detected as an electrical signal near the front side 104 of the sensor substrate 102.

[0021] The sensor substrate 102 may be a substrate with a p-type dopant such as boron or n-type dopant such as phosphorous or arsenic doped by a suitable implantation process, such as a diffusion process. The substrate may be a bulk silicon, any other suitable semiconducting materials such as crystalline germanium, compound semiconductors such as silicon germanium, silicon carbide, gallium arsenide, gallium phosphide, indium phosphide, indium arsenide, gallium phosphide, indium phosphide, indium arsenide, indium antimonide, III-V, III-Nitrides or combinations thereof. Alternatively, the substrate may be a silicon-on-insulator (SOI) substrate that includes a semiconductor layer such as silicon or germanium formed on an insulator layer, formed using wafer bonding and/or other suitable methods. The insulator layer may be a buried oxide (BOX) layer formed in a semiconductor substrate. The substrate may have any suitable crystallographic orientation (e.g., a (100), (110), (111), or (001) crystallographic orientation). The thickness of the substrate may range between about 100 microns (μm) and 1000 μm .

[0022] In the sensor substrate 102, an array or grid of pixels 108 are formed. The pixels 108 may be varied from one another to have different depths, thicknesses, widths, and so forth. Although only two pixels 108 are illustrated in FIG. 1, any number of pixels 108 may be implemented in the sensor substrate 102. The sensor substrate 102 may further include isolation structures 112, which provide electrical and optical isolation between the pixels 108. The isolation structures 112 may be shallow trench isolation (STI) structures that are formed of a dielectric material such as silicon oxide or silicon nitride filled in trenches 114, deep trench isolation (DTI) structures that are formed of a dielectric or polycrystalline materials in the trenches 114, or a capacitor with airgaps in the trenches 114. The trenches 114 are formed by etching the sensor substrate 102. In some embodiments, the isolation structures 112 include doped isolation features, such as heavily doped n-type or p-type regions. Although only three isolation structures 112 are illustrated in FIG. 1, any number of isolation structures may be implemented in the sensor substrate 102 so that the pixels 108 may be

properly isolated. The pixels 108 and the trenches 114 have a depth of between about 3 μm and about 10 μm or beyond. The pixels 108 have a width of between about 1.2 μm and about 1.4 μm and may reduce down to about 0.7 μm or beyond. The isolation structures 112 have a width of between about 50 nm and about 300 nm, having an aspect ratio of between 5 and 100 and possibly beyond.

[0023] The image sensor device 100 further includes a charge layer 116 epitaxially grown conformally directly on surfaces of the pixels 108 on the back side 106 of the sensor substrate 102, including inner walls of the trenches 114. The pixels 108 may include defect centers and a high concentration of dangling bonds near the surfaces of the pixels 108 on the back side 106 of the sensor substrate 102 due to device processing such as etching to form the trenches 114 and thinning of the sensor substrate 102 from the back side 106. Charge carriers generated from the defect centers and the dangling bonds that would cause the generation of noise in the electrical signals converted from photo-energy in the array of pixels 108 are passivated (*i.e.*, recombined) with charge carriers formed in the charge layer 116. Thus, the noise in the electrical signals is reduced. The charge layer 116 may include boron-doped silicon (Si:B), boron-doped silicon germanium (SiGe:B), boron-doped germanium (Ge:B), or a combination thereof. In some embodiments, the charge layer 116 is formed of carbon-doped silicon (Si:C), which blocks metal diffusion from the front side 104 of the sensor substrate 102, in addition to providing the charge carriers. The charge layer 116 formed of silicon germanium (SiGe), germanium (Ge), or carbon-doped silicon (Si:C) on the sensor substrate 102 formed of doped silicon induces tension at the interface with the sensor substrate 102 due to a lattice mismatch, and thus the indirect bandgap of silicon is modified toward a direct bandgap, which enhances generation of electron-hole pairs and therefore the electrical signal. Thickness of the charge layer 116 may be between about 5nm and 50 nm. Since such epitaxial charge layer can also serve as extension of pixel area, which could increase the thickness beyond 50nm depending on integration. A density of formed charge carriers in the charge layer 116 may be between $1 \times 10^{18}/\text{cm}^3$ and $5 \times 10^{21}/\text{cm}^3$.

[0024] The image sensor device 100 may further have an interconnect structure 118 formed over the front side 104 of the sensor substrate 102. The interconnect structure 118 may include a plurality of patterned dielectric layers and conductive layers that

provide interconnections (e.g., wiring) between the various doped features, circuitry, and input/output of the image sensor device 100. The interconnect structure 118 may further include an interlayer dielectric (ILD), a multilayer interconnect (MLI) structure, including, for example, contacts, vias, and metal lines. The MLI structure may include aluminum interconnects formed of aluminum/silicon/copper alloy, titanium, titanium nitride, tungsten, polysilicon, metal silicide, or combinations thereof. Alternatively, the MLI structure may include copper multilayers interconnect formed of copper alloy, titanium, titanium nitride, tantalum, tantalum nitride, tungsten, polysilicon, metal silicide, or combinations thereof.

[0025] FIG. 2 is a cross sectional view of a back-side illuminated (BSI) image sensor device 200 fabricated according to a second embodiment of the present disclosure. In the following description, the same reference numerals are used for the components that are substantially the same as those of the first embodiment, and the description of repeated components may be omitted.

[0026] The image sensor device 200 includes a sensor substrate 102 having a front side 104 and a back side 106.

[0027] In the sensor substrate 102, an array or grid of pixels 108 are formed. The sensor substrate 102 may further include isolation structures 212, which provide electrical and optical isolation between the pixels 108. The isolation structures 212 may be shallow trench isolation (STI) structures that are formed of a dielectric material such as silicon oxide or silicon nitride filled in trenches 214, deep trench isolation (DTI) structures that are formed of a dielectric or polycrystalline materials filled in the trenches 214, or a capacitor with airgaps in the trenches 214. The trenches 214 are formed by etching the sensor substrate 102. In some embodiments, the isolation structures 212 include doped isolation features, such as heavily doped n-type or p-type regions. Although only three isolation structures 212 are illustrated in FIG. 2, any number of isolation structures may be implemented in the sensor substrate 102 so that the pixels 108 may be properly isolated.

[0028] The image sensor device 200 includes an epitaxially grown layer 216 (referred to as an "Epi layer" hereinafter) directly on top surfaces of the pixels 108 on the back side 106 of the sensor substrate 102. The Epi layer 216 may be formed of boron-doped silicon (Si:B), boron-doped silicon germanium (SiGe:B), or boron-doped

germanium (Ge:B), carbon-doped silicon (Si:C). The image sensor device 200 further includes a charge layer 218 over the Epi layer 216 and inner walls of the trenches 214. In some embodiments, the charge layer 218 includes boron-doped silicon (Si:B), boron-doped silicon germanium (SiGe:B), boron-doped germanium (Ge:B), or carbon-doped silicon (Si:C) that is epitaxially grown on the exposed surface of the sensor substrate 102 on the back side 106. In some embodiments, the charge layer 218 is formed by adding a dielectric material on the exposed surface of the sensor substrate 102 on the back side 106 having the opposite type of the desired type of charges, such that the desired type of charges is induced in the substrate near the back side 106.

[0029] FIG. 3 is a flowchart of a method 300 for fabricating an image sensor device, such as a back-side illuminated (BSI) image sensor, 100, according to the first embodiment of the present disclosure. FIGs. 4A-4E schematically illustrate intermediate steps performed in the method 300.

[0030] In block 302 of the method 300, a sensor substrate 102 is provided or fabricated, as shown in FIG. 4A. The sensor substrate 102 may be a photodiode formed of a substrate with a p-type dopant such as boron or n-type dopant such as phosphorous or arsenic doped by a suitable implantation process, such as a diffusion process. The substrate may be a bulk silicon, any other suitable semiconducting materials such as crystalline germanium, compound semiconductors such as silicon germanium, silicon carbide, gallium arsenide, gallium phosphide, indium phosphide, indium arsenide, gallium phosphide, indium phosphide, indium arsenide, indium antimonide, III-V, III-Nitrides or combinations thereof. Alternatively, the substrate may be a silicon-on-insulator (SOI) substrate that includes a semiconductor layer such as silicon or germanium formed on an insulator layer, formed using wafer bonding and/or other suitable methods. The insulator layer may be a buried oxide (BOX) layer formed in a semiconductor substrate. The substrate may have any suitable crystallographic orientation (e.g., a (100), (110), (111), or (001) crystallographic orientation). The thickness of the substrate may range between about 100 microns (μm) and 1000 μm .

[0031] In block 304 of the method 300, an interconnect structure 118 is formed over the front side 104 of the sensor substrate 102, as shown in FIG. 4B. The interconnect structure 118 may include a plurality of patterned dielectric layers and conductive layers that provide interconnections (e.g., wiring) between the various doped features,

circuitry, and input/output of the image sensor device 100. The interconnect structure 118 may further include an interlayer dielectric (ILD), a multilayer interconnect (MLI) structure, including, for example, contacts, vias, and metal lines. The MLI structure may include aluminum interconnects formed of aluminum/silicon/copper alloy, titanium, titanium nitride, tungsten, polysilicon, metal silicide, or combinations thereof. Aluminum interconnects may be formed by a process, for example, physical vapor deposition (PVD) (or sputtering), chemical vapor deposition (CVD), atomic layer deposition (ALD), photolithography processing, etching to pattern the conductive materials for vertical connection (for example, vias/contacts) and horizontal connection (for example, conductive lines), or combinations thereof. Alternatively, the MLI structure may include copper multilayers interconnect formed of copper alloy, titanium, titanium nitride, tantalum, tantalum nitride, tungsten, polysilicon, metal silicide, or combinations thereof. The copper interconnect structure may be formed by a process, for example, CVD, sputtering, plating, or other suitable processes.

[0032] In block 306 of the method 300, the sensor substrate 102 is flipped over and thinned from the back side 106, as shown in FIG. 4C. The sensor substrate 102 is thinned such that charge carriers induced near the back side 106 of the sensor substrate 102 diffuse to the front side 104. The thinning process may include a mechanical grinding process and a chemical thinning process. The mechanical grinding process may first remove substantial amount of substrate material from the sensor substrate 102, and then the chemical thinning process may apply an etching chemical to the back side 106 of the sensor substrate 102 to further thin the sensor substrate 102 to a desired thickness. When the sensor substrate 102 is a SOI type, an imbedded buried oxide layer (BOX) can act as an etching stop layer. A desired thickness of the sensor substrate 102 may vary depending on type of applications and design requirements of the image sensor device, between about 3 μm and about 10 μm .

[0033] In block 308 of the method 300, trenches 114 are etched into the sensor substrate 102 from the back side 106. Pixels 108 are each defined between two adjacent trenches 114 and an array or grid of pixels 108 are formed. The pixels 108 may be varied from one another to have different depths, thicknesses, widths, and so forth. Although only two pixels 108 and three trenches 114 are illustrated in FIG.

4D, any number of pixels 108 or trenches 114 may be implemented in the sensor substrate 102. The pixels 108 and the trenches 114 have a depth of between about 3 μm and about 10 μm . The pixels 108 have a width of between about 0.7 μm and about 2.5 μm and may reduce down to about 0.5 μm . The trenches 114 have a width of between about 50 nm and about 300 nm, having an aspect ratio of between 50 and 100.

[0034] In block 310 of the method 300, an exposed surface of the sensor substrate 102 on the back side 106 is pre-cleaned to remove organic materials, native oxides such as carbon oxide and other impurities, to enhance performance of the image sensor device 100. A cleaning solution may include a mixture of H_2O_2 - H_2SO_4 and/or wet oxidation, dry oxidation and an aqueous HF (hydrofluoric acid). The cleaned surface of the sensor substrate 102 may be dried by a drier to remove any residual liquids or particles. In some embodiments, the pre-cleaning process is performed at a low temperature, about 450°C or less.

[0035] In block 312 of the method 300, a charge layer 116 is epitaxially grown on the exposed surface of the sensor substrate 102 on the back side 106, including inner walls of the trenches 114 (that is, exposed surfaces of the pixels 108), as shown in FIG. 4E. The charge layer 116 may include boron-doped silicon (Si:B), boron-doped silicon germanium (SiGe:B), boron-doped germanium (Ge:B), or carbon-doped silicon (Si:C). The epitaxial growth of the charge layer 116 is performed by supplying a source gas containing a silicon source (e.g., SiH_4 or SiHCl_3) and a dopant such as a boron compound (e.g., diborane; B_2H_6) at a low temperature, about 450°C or less, to ensure the protection of metal interconnect in wafer front side and the implanted dopants in the sensor substrate 102 not to migrate or be deactivated within sensor substrate 102, which may harm the sensor substrate 102. Due to the nature of the epitaxial growth, the charge layer 116 passivates dangling bonds on the exposed surface and conformally covers the surfaces of the pixels 108 on the back side 106, including the inner walls of the trenches 114. Charge carriers are activated from the dopants (such as boron) as the charge layer 116 is epitaxially grown, without the need for activation anneal as in the case for activating charges from implanted dopants. A density of charge carriers activated from the dopant (such as boron) in the charge layer 116 may be between $1 \times 10^{18}/\text{cm}^3$ and $5 \times 10^{21}/\text{cm}^3$. Charge carrier activated in the charge layer

116 passivate (*i.e.*, recombine with) charge carriers induced at defect centers and dangling bonds near the surfaces of the pixels 108, including inner walls of the trenches 114. Those defect centers and dangling bonds are caused by device processing such as the thinning process in block 306 and the etching process in block 308. Thickness of the charge layer 116 may be between about 5 nm and 50 nm. The charge layer 116 provides the same function of an etch stop layer as the BOX in a SOI type in addition to other functions such as passivation, stress engineering, bandpass filter, or the like. In both a SOI type and the charge layer 116 on the handle substrate 602, total thickness variation (TTV) is therefore determined by deposition processes instead of removal processes.

[0036] In block 314 of the method 300, isolation structures 112 are formed as shown in FIG. 1, by filling the trenches 114 with a dielectric material such as silicon oxide or silicon nitrides or polymetallic materials, or forming capacitors with airgaps. In some embodiments, the isolation structures 112 may include heavily doped n-type or p-type regions. The isolation structures 112 provide electrical and optical isolation between the pixels 108.

[0037] It should be noted that the particular example embodiments described above are just some possible example methods of fabricating semiconductor devices having integrated circuits according to the present disclosure and do not limit the possible configurations, specifications, or the like of liquid ejecting devices according to the present disclosure. For example, the methods can be applied to fabricate other semiconductor devices such as solar cells. Further, the order of the blocks of the method 300 can be replaced and some of the blocks of the method 300 can be repeated or omitted. The trenches 114 can be etched from the front side 104 of the sensor substrate 102.

[0038] FIG. 5 is a flowchart of a method 500 for fabricating an image sensor device, such as a back-side illuminated (BSI) image sensor device, 200, according to the second embodiment of the present disclosure. FIGS. 6A-6F schematically illustrate intermediate steps performed in the method 500. In the following description, the same reference numerals are used for the components that are substantially the same as those of the first embodiment, and the description of repeated components may be

omitted. Further, the method 500 according the second embodiment may be combined with the method 300 according to the first embodiment.

[0039] In block 502 of the method 500, a layer 216 is epitaxially grown on a handle substrate 602, as shown in FIG. 6A. The epitaxially grown layer 216 (referred to as an “Epi layer” hereinafter) may include charges or may not include charges. The handle substrate 602 may be silicon wafer, Ge wafer, SOI wafer, III-V wafer with p-type dopant such as boron or n-type dopant such as phosphorous, arsenic, etc. or intrinsic. The Epi layer 216 may include boron-doped silicon (Si:B), boron-doped silicon germanium (SiGe:B), boron-doped germanium (Ge:B), or carbon-doped silicon (Si:C). The epitaxial growth of the Epi layer 216 is performed by supplying a source gas containing a silicon source (e.g., SiH_4 or SiHCl_3) and a dopant such as a boron compound (e.g., diborane; B_2H_6) at a temperature of between about 500°C and about 900°C . A density of charge carriers activated from the dopant (such as boron) in the Epi layer 216 may be between $1 \times 10^{17}/\text{cm}^3$ and $5 \times 10^{21}/\text{cm}^3$. Thickness of the Epi layer 216 may be between about 5 nm and 100 nm.

[0040] In block 504 of the method 500, a semiconductor layer 604 is epitaxially grown over the Epi layer 216, as shown in FIG. 6B. The semiconductor layer 604 may be a single semiconducting material such as silicon or germanium or a compound semiconductor, such as silicon germanium, gallium arsenic, gallium phosphide, indium phosphide, indium arsenide, and/or indium antimonide, III-V, III-Nitrides; or combinations. The semiconductor layer 604 may be a silicon-on-insulator (SOI) substrate that include a semiconductor layer such as silicon or germanium formed on an insulator layer using wafer bonding, and/or other suitable methods. The insulator layer may be formed of any suitable material, including silicon oxide, sapphire, other suitable insulating materials, and/or combinations thereof. An exemplary insulator layer may be a buried oxide layer (BOX) or epitaxial oxide/silicon stacking. The insulator layer is formed by any suitable process, such as separation by implantation of oxygen (SIMOX), oxidation, deposition, and/or other suitable process. The substrate may have any suitable crystallographic orientation (e.g., a (100), (110), (111), or (001) crystallographic orientation). The thickness of the semiconductor layer 604 may range between about 100 microns (μm) and 1000 μm .

[0041] In block 506 of the method 500, a p-type dopant such as boron and n-type dopant such as phosphorous or arsenic is doped into the semiconductor layer 604 by a suitable implantation process 606, such as a diffusion or an epitaxial process to form a sensor substrate 102, as shown in FIG. 6C. A front side 104 of the sensor substrate 102 is exposed and a back side 106 of the sensor substrate 102 is in direct contact with the Epi layer 216.

[0042] In block 508 of the method 500, an interconnect structure 118 is formed over the front side 104 of the sensor substrate 102 as in block 304.

[0043] In block 510 of the method 500, the sensor substrate 102 is flipped over and the handle substrate 602 is removed from the Epi layer 216, as shown in FIG. 6D. The handle substrate 602 can be removed by grinding, chemical polishing and wet or dry etching/cleaning. In some embodiments, the Epi layer 216 is formed of material that is with different composition from the handle substrate 602, such as SiGeB, SiGeBC, Si:C, Si:B, Si:P, Si:PC, SiAs,. Due to a different material etching rate between the handle substrate 602 and the Epi layer 216, the etching process stops at the Epi layer 216.

[0044] In block 512 of the method 500, trenches 214 are etched into the sensor substrate 102 from the back side 106. Pixels 108 are each defined between two adjacent trenches 214 and an array or grid of pixels 108 are formed. The pixels 108 may be varied from one another to have different depths, thicknesses, widths, and so forth. Although only two pixels 108 and three trenches 214 are illustrated in FIG. 6E, any number of pixels 108 or trenches 214 may be implemented in the sensor substrate 102. The trenches 214 have a width of between about 50 nm and about 300 nm, having an aspect ratio of between 10 and 100.

[0045] In block 514 of the method 500, a charge layer 218 is formed over the exposed surface of the sensor substrate 102 on the back side 106, including inner walls of the trenches 214, as shown in FIG. 6F. In some embodiments, the charge layer 218 includes boron-doped silicon (Si:B), boron-doped silicon germanium (SiGe:B), boron-doped germanium (Ge:B), or carbon-doped silicon (Si:C) that is epitaxially grown after the exposed surface of the sensor substrate 102 on the back side 106 is pre-cleaned as in block 310 of the method 300. In some embodiments, the charge layer 218 is

formed by adding a dielectric material on the exposed surface of the sensor substrate 102 on the back side 106 having the opposite type of the desired type of charges, such that the desired type of charges is induced in the substrate near the back side 106.

[0046] In block 516 of the method 500, isolation structures 212 are formed as shown in FIG. 2, by filling the trenches 214 with a dielectric material such as silicon oxide or silicon nitrides or polycrystalline materials, or forming capacitors with airgaps. In some embodiments, the isolation structures 212 may include heavily doped n-type or p-type regions. The isolation structures 212 provide electrical and optical isolation between the pixels 108.

[0047] It should be noted that the particular example embodiments described above are just some possible example methods of fabricating semiconductor devices having integrated circuits according to the present disclosure and do not limit the possible configurations, specifications, or the like of liquid ejecting devices according to the present disclosure. For example, the methods can be applied to fabricate other semiconductor devices such as solar cells. Further, the order of the blocks of the method 500 can be replaced and some of the blocks of the method 500 can be repeated or omitted. The trenches 214 can be etched from the front side 104 of the sensor substrate 102.

[0048] In the example embodiments described above, the image sensors and the methods for fabricating the same are provided to reduce noise in the electrical signals converted from photo-energy in array of pixels. An epitaxially grown charge layer in the image sensors provide a large concentration of charge carriers to passivate excess charge carriers generated at surfaces of pixels in the image sensors. An epitaxially grown charge layer may provide additional functions such as an etch stop layer in a fabrication process or a getter that blocks metal diffusion within the image sensors and/or the stress to engineer the material bandgap/work function near sensor surfaces and/or the separation between signal and noise.

[0049] While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms. Furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from

the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

What is claimed is:

1. A method of fabricating a semiconductor device, comprising:
forming an interconnect structure over a front side of a sensor substrate;
thinning the sensor substrate from a back side of the sensor substrate;
etching trenches into the sensor substrate;
pre-cleaning an exposed surface of the sensor substrate;
epitaxially growing a charge layer directly on the pre-cleaned exposed surface
of the sensor substrate; and
forming isolation structures within the etched trenches.
2. The method of claim 1, wherein the sensor substrate is a silicon photodiode.
3. The method of claim 1, wherein the charge layer comprises a material selected
from boron-doped silicon, boron-doped silicon germanium, and boron-doped
germanium.
4. The method of claim 3, wherein a density of charge carriers in the charge layer
is between $1 \times 10^{18}/\text{cm}^3$ and $5 \times 10^{21}/\text{cm}^3$.
5. The method of claim 1, wherein the charge layer has a thickness of between
5nm and 50nm.
6. The method of claim 1, wherein the epitaxial growth of the charge layer is
performed at a temperature of 450°C or less.
7. The method of claim 1, wherein the dielectric material is selected from silicon
oxide and silicon nitride.
8. A method of fabricating a semiconductor device, comprising:
epitaxially growing a layer directly on a surface of a handle substrate;
epitaxially growing a semiconductor layer directly on the epitaxially grown layer;

implanting a dopant into the semiconductor layer;
etching trenches into the semiconductor layer;
forming isolation structures within the etched trenches;
forming an interconnect structure over the semiconductor layer; and
removing the handle substrate from the epitaxially grown layer.

9. The method of claim 8, wherein:
the semiconductor layer comprises silicon,
a dopant comprises boron, phosphorous, or arsenide, and
the dielectric material is selected from silicon oxide and silicon nitride.
10. The method of claim 8, wherein the charge layer comprises a material selected from boron-doped silicon, boron-doped silicon germanium, and boron-doped germanium.
11. The method of claim 10, wherein a density of charge carriers in the charge layer is between $1 \times 10^{17}/\text{cm}^3$ and $5 \times 10^{21}/\text{cm}^3$.
12. The method of claim 8, wherein the charge layer has a thickness of between 5nm and 100nm.
13. The method of claim 8, wherein the epitaxial growth of the charge layer is performed at a temperature of between 500°C and about 900°C.
14. An image sensor, comprising:
a sensor substrate having a front side and a back side;
a plurality of pixels formed within the sensor substrate on the back side;
a plurality of isolation structures formed within the sensor substrate, wherein the plurality of pixels are isolated from each other by one of the plurality of isolation structures;
an interconnect structure over the front side of the sensor substrate; and
a charge layer epitaxially grown directly on surfaces of the plurality of pixels on the back side of the sensor substrate.

15. The image sensor of claim 14, wherein the sensor substrate is a silicon photodiode.
16. The image sensor of claim 14, wherein the charge layer comprises a material selected from boron-doped silicon, boron-doped silicon germanium, and boron-doped germanium.
17. The image sensor of claim 16, wherein a density of charge carriers in the charge layer is between $1 \times 10^{18}/\text{cm}^3$ and $5 \times 10^{21}/\text{cm}^3$.
18. The image sensor of claim 14, wherein the charge layer has a thickness of between 5nm and 50nm.
19. The image sensor of claim 14, wherein the plurality of isolation structures comprise a silicon-containing dielectric material.
20. The image sensor of claim 14, wherein the plurality of isolation structures each have an aspect ratio of a width to a depth of between 50 and 100.