What is claimed:

1. A method of forming a DRAM comprising the steps of:

providing a substrate having device isolation structures formed thereon, an active device region defined between the device isolation structures;

providing an insulating layer on the substrate over the active device region;

providing a first and second transfer transistor on the active device region, the first transfer transistor including a first gate electrode over the insulating layer, and first and second source/drain regions formed in the substrate, the second transfer transistor including a second gate electrode over the insulating layer, the second source/drain region and a third source/drain region formed in the substrate, the first and second transfer transistors sharing the second source/drain region;

forming an ~~etch stop~~ silicon nitride layer over the first and second gate electrodes and over the first, second and third source/drain regions;

forming a ~~dielectric~~ silicon oxide layer over the ~~etch stop~~ silicon nitride layer, the dielectric layer being different from the etch stop layer;

etching through the ~~dielectric~~ silicon oxide layer above the second source/drain region, stopping the etching process on the ~~etch stop~~ silicon nitride layer, performing a further etching process to etch through the ~~etch stop~~ silicon nitride layer and then forming a bit line contact to the second source/drain region; and

etching through the ~~dielectric~~ silicon oxide layer above the third source/drain region, stopping the etching process on the ~~etch stop~~ silicon nitride layer, performing a further etching process to etch through the ~~etch stop~~ silicon nitride layer and then forming a charge storage capacitor having an electrode connected to the third source/drain region.

2. The method of claim 1, further comprising the step of planarizing a surface of the ~~dielectric~~ silicon oxide layer prior to the step of etching through the ~~dielectric~~ silicon oxide layer above the third source/drain region.

3. The method of claim 2, wherein the step of planarizing is accomplished using chemical mechanical polishing.

4. The method of claim 2, wherein the step of planarizing is performed prior to the step of etching through the ~~dielectric~~ Silicon oxide layer above the second source/drain region.

~~5. The method of claim 1, wherein the dielectric layer is an oxide of silicon and the etch stop layer is silicon nitride.~~ ~~silicon oxide~~

6. The method of claim 1, wherein the ~~etch stop~~ silicon nitride layer is formed in contact with the first, second and third source/drain regions.

7. The method of claim 6, wherein the ~~etch stop~~ silicon nitride layer is separated from the first and second gate electrodes by a layer of oxide.

~~8. The method of claim 6, wherein the etch stop layer is silicon nitride and the dielectric is an oxide of silicon.~~

9. A method of forming a DRAM comprising the steps of:

providing a substrate having device isolation structures formed thereon, an active device region defined between the device isolation structures;

providing an insulating layer on the substrate over the active device region;

providing a transfer transistor on the active device region, the transfer transistor including a first gate electrode over the insulating layer, and first and second source/drain regions formed in the substrate;

forming an etch stop layer over the first gate electrode and over the first and second source/drain regions;

forming a dielectric layer over the etch stop layer, the dielectric layer being different from the etch stop layer;

planarizing the surface of the dielectric layer by using CMP to provide a planarized surface;

etching through the planarized surface of the dielectric layer above the first source/drain region, stopping the etching process on the etch stop layer, performing a further etching process to etch through the etch stop layer and then forming a bit line contact to the first source/drain region; and

etching through the planarized surface of the dielectric layer above the second source/drain region, stopping the etching process on the etch stop layer, performing a further etching process to etch through the etch stop layer and then forming a charge storage capacitor having an electrode connected to the second source/drain region.

10. The method of claim 9, wherein the step of forming a dielectric layer includes chemical vapor deposition from a TEOS source gas.

~~11. The method of claim 10, wherein the step of planarizing is accomplished using chemical mechanical polishing.~~

12. The method of claim 9, wherein the dielectric layer is an oxide of silicon and the etch stop layer is silicon nitride.

13. The method of claim 12, wherein the etch stop layer is formed on the first and second source/drain regions.

14. A method of forming a DRAM comprising the steps of:

providing a substrate having device isolation structures formed thereon, an active device region defined between the device isolation structures;

providing an insulating layer on the substrate over the active device region;

providing a transfer transistor on the active device region, the transfer transistor including a first gate electrode over the insulating layer, and first and second source/drain regions formed in the substrate;

forming an ~~etch stop~~ silicon nitride layer over the first gate electrodes and on an first oxide layer covering the first and second source/drain regions;

providing a ~~dielectric~~ second oxide layer over the ~~etch stop~~ silicon nitride layer; ~~wherein the dielectric layer is different from the etch stop layer, and wherein the etch stop layer is different from the oxide layers~~ silicon nitride

chemical mechanical polishing the surface of the ~~dielectric~~ second oxide layer to provide a planarized surface; and

etching through the planarized surface of the ~~dielectric~~ second oxide layer above the first source/drain regions, stopping the etching process on the ~~etch stop~~ silicon nitride layer, performing a further etching process to etch through the ~~etch stop~~ silicon nitride layer, removing the oxide first layer to expose at least a portion of the first source/drain region and then providing a conductor in contact with the one source/drain region.

What is claimed:

1. A method of forming a DRAM comprising the steps of:

providing a substrate having device isolation structures formed thereon, an active device region defined between the device isolation structures;

providing an insulating layer on the substrate over the active device region;

providing a first and second transfer transistor on the active device region, the first transfer transistor including a first gate electrode over the insulating layer, and first and second source/drain regions formed in the substrate, the second transfer transistor including a second gate electrode over the insulating layer, the second source/drain region and a third source/drain region formed in the substrate, the first and second transfer transistors sharing the second source/drain region;

forming an ~~etch stop~~ silicon nitride layer over the first and second gate electrodes and over the first, second and third source/drain regions;

forming a ~~dielectric~~ silicon oxide layer over the ~~etch stop~~ silicon nitride layer, the dielectric layer being different from the etch stop layer;

etching through the ~~dielectric~~ silicon oxide layer above the second source/drain region, stopping the etching process on the ~~etch stop~~ silicon nitride layer, performing a further etching process to etch through the ~~etch stop~~ silicon nitride layer and then forming a bit line contact to the second source/drain region; and

etching through the ~~dielectric~~ silicon oxide layer above the third source/drain region, stopping the etching process on the ~~etch stop~~ silicon nitride layer, performing a further etching process to etch through the ~~etch stop~~ silicon nitride layer and then forming a charge storage capacitor having an electrode connected to the third source/drain region.

2. The method of claim 1, further comprising the step of planarizing a surface of the ~~dielectric~~ Silicon Oxide layer prior to the step of etching through the ~~dielectric~~ silicon oxide layer above the third source/drain region.

3. The method of claim 2, wherein the step of planarizing is accomplished using chemical mechanical polishing.

4. The method of claim 2, wherein the step of planarizing is performed prior to the step of etching through the ~~dielectric~~ Silicon oxide layer above the second source/drain region.

~~5. The method of claim 1, wherein the dielectric layer is an oxide of silicon and the etch stop layer is silicon nitride.~~ ~~silicon oxide~~

6. The method of claim 1, wherein the ~~etch stop~~ silicon nitride layer is formed in contact with the first, second and third source/drain regions.

7. The method of claim 6, wherein the ~~etch stop~~ silicon nitride layer is separated from the first and second gate electrodes by a layer of oxide.

~~8. The method of claim 6, wherein the etch stop layer is silicon nitride and the dielectric is an oxide of silicon.~~

9. A method of forming a DRAM comprising the steps of:

providing a substrate having device isolation structures formed thereon, an active device region defined between the device isolation structures;

providing an insulating layer on the substrate over the active device region;

providing a transfer transistor on the active device region, the transfer transistor including a first gate electrode over the insulating layer, and first and second source/drain regions formed in the substrate;

forming an etch stop layer over the first gate electrode and over the first and second source/drain regions;

forming a dielectric layer over the etch stop layer, the dielectric layer being different from the etch stop layer;

planarizing the surface of the dielectric layer by using CMP to provide a planarized surface;

etching through the planarized surface of the dielectric layer above the first source/drain region, stopping the etching process on the etch stop layer, performing a further etching process to etch through the etch stop layer and then forming a bit line contact to the first source/drain region; and

etching through the planarized surface of the dielectric layer above the second source/drain region, stopping the etching process on the etch stop layer, performing a further etching process to etch through the etch stop layer and then forming a charge storage capacitor having an electrode connected to the second source/drain region.

10. The method of claim 9, wherein the step of forming a dielectric layer includes chemical vapor deposition from a TEOS source gas.

~~11. The method of claim 10, wherein the step of planarizing is accomplished using chemical-mechanical polishing.~~

12. The method of claim 9, wherein the dielectric layer is an oxide of silicon and the etch stop layer is silicon nitride.

13. The method of claim 12, wherein the etch stop layer is formed on the first and second source/drain regions.

14. A method of forming a DRAM comprising the steps of:

providing a substrate having device isolation structures formed thereon, an active device region defined between the device isolation structures;

providing an insulating layer on the substrate over the active device region;

providing a transfer transistor on the active device region, the transfer transistor including a first gate electrode over the insulating layer, and first and second source/drain regions formed in the substrate;

forming an ~~etch stop~~ silicon nitride layer over the first gate electrodes and on an first oxide layer covering the first and second source/drain regions;

providing a ~~dielectric~~ second oxide layer over the ~~etch stop~~ silicon nitride layer; ~~wherein the dielectric layer is different from the etch stop layer, and wherein the etch stop layer is different from the oxide layer;~~ silicon nitride

chemical mechanical polishing the surface of the ~~dielectric~~ second oxide layer to provide a planarized surface; and

etching through the planarized surface of the ~~dielectric~~ second oxide layer above the first source/drain regions, stopping the etching process on the ~~etch stop~~ silicon nitride layer, performing a further etching process to etch through the ~~etch stop~~ silicon nitride layer, removing the first oxide layer to expose at least a portion of the first source/drain region and then providing a conductor in contact with the one source/drain region.