

HIGHLY INTEGRATED SEMICONDUCTOR MEMORY DEVICE
AND METHOD OF MANUFACTURE THEREFOR

The present invention relates to a semiconductor memory device and a manufacturing method therefor, and particularly to a highly integrated semiconductor memory device and a manufacturing method therefor wherein the effective area of a capacitor can be maximized without expanding the memory cell areas.

In the field of the semiconductor memory techniques, competitive efforts have been carried out to increase the number of memory cell in a chip. In order to achieve this object, it is important to minimize the area of a memory cell array, on which a plurality of memory cells are formed within a restricted surface of a chip.

In realizing a minimum area for the memory cell, a DRAM (Dynamic Random Access Memory) of which individual cells have a single transistor and a single capacitor is well known. In this memory cell since a large portion of the area is occupied by the capacitor with the development of higher packing density of the highly integrated semiconductor memory device, it has become more important to increase the capacitance of the capacitor along with minimizing the ratio of the semiconductor area occupied by the capacitor, so as to facilitate information detection and to decrease soft errors resulting from alpha particles.

In order to minimize the area occupied by a capacitor and maximize the capacitance of a storage capacitor as

described above, a spread stacked capacitor (to be called hereinafter SSC) cell structure, in which the storage electrode of each memory cell extends to the adjacent memory cell area, has been proposed. Such a conventional memory cell having the SSC cell structure was disclosed in pages 31 to 34 of IEDM 89.

In the prior art mentioned above, first electrodes of the capacitor are formed to extend to the areas of adjacent memory cells by exposing the source region of each memory cell on a semiconductor silicon substrate in which transistors are formed. A 64Mbit DRAM can be achieved in the aforesaid structure of the SSC cell. However, there is a limitation in obtaining sufficient storage area for the capacitor required for a 256Mbit DRAM, because a first capacitor should be formed between second capacitors which are formed afterwards. That is, since the size of each capacitor of the first memory cells is restricted by each capacitor of the second memory cells, the extension of the capacitors of the second memory cells which are expanded to the left and right, should be restricted in order to keep in balance with the size of each capacitor of the first memory cells. Accordingly, each capacitor of the second memory cells could not be fully expanded to the capacitor of the first memory cells disposed adjacent to the second memory cells to overlap in maximum areas with the first memory cells. The size of each capacitor of the first memory cells should be enlarged to maintain balance with those of the capacitors of the first memory cells as well as to expand fully each capacitor of the second memory cells to the capacitor of the adjacent first memory cells. However, because the size of

each capacitor of the first memory cells is restricted by each capacitor of the second memory cells in the conventional SSC cell structure, it is insufficient to obtain the effective area of the capacitor required for the 256Mbit DRAM of which cell size is smaller than that of the 64Mbit DRAM.

Therefore, it is an object of the present invention to provide a DRAM, wherein, to solve the above described problems of the conventional techniques, a memory cell array is formed by alternately disposing a stack capacitor cell and a combined stack-trench capacitor cell adjacent to each other.

It is another object of the present invention to provide a manufacturing method which effectively manufactures the DRAM having the above mentioned structure.

According to the present invention there is provided a highly integrated semiconductor memory device comprising first and second pluralities of memory cells, each memory cell of said first plurality of memory cells including a first switching transistor formed on a semiconductor substrate and a first capacitor coupled to said first switching transistor, each memory cell of said second plurality of memory cells including a second switching transistor formed on said semiconductor substrate and a second capacitor coupled to said second switching transistor, and each of said first and second pluralities of memory cells being alternately disposed in each of a plurality of rows,

wherein each said first capacitor comprises a first storage electrode including a trench portion formed partially in said substrate and a first stack portion, and said first

stack portion has overlap portions each extended to overlap a portion of adjacent second memory cells, and

wherein each said second capacitor comprises a second storage electrode including only a second stack portion and thus not including a trench portion partially formed in said substrate, wherein said second stack portion has a contact portion and also has overlap portions, each overlap portion extending to overlap an overlap portion of said first stack portion of adjacent first memory cells.

Preferably the respective first and second memory cells are disposed alternately and adjacent one another in row direction and in column direction.

According to a further aspect of the present invention there is provided a method for manufacturing a highly integrated semiconductor memory device comprising in the recited order the steps of:

defining active regions by growing field oxide layers on a first conductivity type semiconductor substrate;

forming transistors, which are elements of a memory cell, on said active regions, and forming a first insulating layer over the resultant structure;

forming bit lines so as to be connected to respective drain regions of said transistors, and forming a second insulating layer over the resultant structure;

forming first openings by exposing predetermined portions of the source regions so as to form first memory cells having a capacitor with a trench portion and a first stack portion;

forming trenches in the semiconductor substrate by using said first openings;

forming capacitors both on the surface of said trenches and on said second insulating layer, and forming a third insulating layer on the resultant structure;

forming second openings in order to expose source regions of the transistors disposed adjacent said first memory cells in both row and column directions; and

forming capacitors with second stack portions through said second openings.

Embodiments of the present invention will now be described, by way of example with reference to the accompanying drawings, in which :

Figure 1 is a partially sectional view of the memory cell according to an embodiment of the present invention;

Figures 2A to 2G illustrate one embodiment of a method for manufacturing a memory cell array according to an embodiment of the present invention of the type shown in Figure 1; and

Figures 3A to 3E illustrate another embodiment of a method for manufacturing a memory cell array according to another embodiment of the present invention.

In the embodiment of the memory cell array shown in Figure 1, memory cells M1 and M3 including combined stack-trench type capacitors 11, 12 and 13, are disposed alternately and adjacent to a memory cell M2 having a stack capacitor 20, 21 and 22. In the memory cells, storage electrodes 11 (first electrodes of the capacitors) of the first and the third memory

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cells M1 and M3 extend to the adjacent second memory cell area, and a storage electrode 20 of the second memory cell M2 extends to the areas of the first and the third memory cells M1 and M3, as well. Although the memory cell array shown in Figure 1 is illustrated as having the memory cells disposed adjacent one another in row direction, the memory cell array in the column direction also has memory cells having the combined stack-trench capacitor and the memory cells having the stack capacitor disposed adjacent one another.

Figures 2A to 2G illustrate one embodiment of processes for manufacturing a memory cell array according to an embodiment of the present invention.

Figure 2A illustrates a process for forming transistors and bit lines 5 on a semiconductor substrate 100, wherein active regions are first defined by growing field oxide layers 101 in a first conductivity type semiconductor substrate 100 by selective oxidation. Impurity-doped first polycrystalline silicon layers which are to be gate electrodes 1 are formed on the active regions by interposing gate oxide layers and, at the same time, first conductive layers 4 of the transistors, e.g., impurity-doped first polycrystalline silicon layers, are formed on any predetermined portions of the field oxide layers 101 such that they are connected to the gate electrodes of the memory cell disposed adjacent the field oxide layers. Source region 2 and drain region 3 are formed on each side of the gate electrodes 1 in the surface of the semiconductor substrate through ion implantation, and then, a first insulating layer I1, e.g., HTO (High Temperature Oxide) layer or LTO (Low Temperature Oxide) layer having a thickness of about 500Å ~ 2000Å, is formed over the entire surface of the aforesaid structure. Thereafter, metal layers 5 serving as bit lines are formed after exposing some portions of the drain regions. Here, the structure of Figure 2A includes the first, the second and the third memory cells M1, M2 and M3.

Figure 2B illustrates a process for forming a second insulating layer I2 and first openings OP1, wherein, after the process shown in Figure 2A, the second insulating layer I2

having a thickness of about $500\text{\AA} \sim 3000\text{\AA}$, e.g., HTO layer, is deposited, and, by using a mask pattern on the second insulating layer, the first openings OP1 are formed to expose the source regions 2 of the first and the third memory cells M1 and M3.

Figure 2C illustrates a process for forming trenches 10 and second conductive layers 11 which function as first electrodes of the capacitors. Through the first openings OP1, the semiconductor substrate 100 is etched to form the trenches 10, thereafter, second conductive layers 11 serving as the first electrodes of the capacitors, e.g., an impurity-doped second polycrystalline silicon layers having a thickness of about $200\text{\AA} \sim 3000\text{\AA}$, are deposited both on the walls of the trenches 10 and on the second insulating layers I2, thereby forming an electrode pattern as shown in Figure 2C. Here, the depth of the trench 10 can be adjusted in the range of about $0.5\mu\text{m} \sim 10\mu\text{m}$, in accordance with the intended value of the capacitance.

Figure 2D illustrates a process for forming dielectric films 12 and third conductive layers 13 serving as the second electrodes of the capacitors. The dielectric films 12 and the third conductive layers 13 having a thickness of about $500\text{\AA} \sim 4000\text{\AA}$ are successively formed, thereby completing the first memory cells M1 and M3 respectively having the combined stack-trench capacitors. Here, the dielectric film 12 is of an oxide layer structure such as HTO layer or LTO layer or an oxide/nitride/oxide structure, i.e., ONO structure, or a nitride/oxide structure, i.e., NO structure. Here, instead

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of the combined stack-trench capacitor, an outside trench capacitor, in which the charge is stored in the outside region of the trench in the semiconductor substrate, can be formed.

Figure 2E illustrates a process for forming third insulating layers I3 and a second opening OP2. After the process shown in Figure 2D, the third insulating layer I3 having a thickness of about $500\text{\AA} \sim 3000\text{\AA}$, e.g., HTO layer, is deposited, and then, the second opening OP2 is formed to expose the source region 2 of the second memory cell M2. Here, after depositing BPSG (Boro-Phosphorus Silicate Glass) layer having a thickness of about $500\text{\AA} \sim 4000\text{\AA}$, the third insulating layer can be formed by planarizing via reflow process.

Figure 2F illustrates a process for forming a fourth conductive layer 20 serving as a first electrode, a dielectric film 21, and a fifth conductive layer 22 serving as a second electrode of the capacitor. After performing the process shown in Figure 2E, the fourth conductive layer 20 having a thickness of about $300\text{\AA} \sim 4000\text{\AA}$, which serves as the first electrode of the capacitor, e.g., impurity-doped fourth polycrystalline silicon layer, is deposited to form the electrode pattern as illustrated in Figure 2F. Thereafter, the dielectric film 21 and the fifth conductive layer 22 having a thickness of about $500\text{\AA} \sim 4000\text{\AA}$ which functions as the second electrode of the capacitor are successively formed over the fourth conductive layer 20, thereby completing the second memory cell M2 having the stack capacitor. Here, the dielectric film 21 is of an oxide layer structure such as HTO layer or LTO layer, of ONO structure, or of NO structure.

Figure 2G illustrates a process for forming a planarizing layer 30 and metal electrodes 31, wherein, after the process shown in Figure 2F, the planarizing layer 30, e.g., BPSG layer, is deposited for planarizing, and then, the metal electrodes 31 are formed, thereby completing the DRAM having both stack-trench capacitor cells and stack capacitor cells.

Figures 3A to 3E show another embodiment of the processes for manufacturing memory cell array according to a further embodiment of the present invention.

The manufacturing process preceding the process of Figure 3A is identical to that described in relation, to Figure 2A and thus is omitted.

Figure 3A illustrates a process for forming a second insulating layer I2, a nitride layer N, and a fourth insulating layer I4. After the process illustrated in Figure 2A, the second insulating layer I2 having a thickness of about $500\text{\AA}$ ~ $3000\text{\AA}$, e.g., HTO layer, the nitride layer N having a thickness of about $100\text{\AA}$ ~ $500\text{\AA}$, and the fourth insulating layer I4 having a thickness of about $500\text{\AA}$ ~ $4000\text{\AA}$, e.g., HTO layer, are sequentially formed.

Figure 3B illustrates a process for forming second conductive layers 11 serving as first electrodes of the capacitors and an inter-planarizing layer 32, wherein, by applying a mask pattern on the fourth insulating layer I4, first openings are formed so as to expose source regions 2 of the first and the third memory cells M1 and M3. The semiconductor substrate is etched to form trenches 10 through

the first openings and, thereafter, second conductive layers 11 having a thickness of about $200\text{\AA} \sim 3000\text{\AA}$, which serve as the first electrodes of the capacitors, e.g., impurity-doped second polycrystalline silicon layers, are deposited to form the electrode pattern as shown in Figure 3B. The inter-planarizing layer 32, e.g., SOG (spin on glass) layer, is deposited to planarize. During the process, the inter-planarizing layer 32 may be formed of a layer stacked by SOG layer and HTO layer or a layer stacked by BPSG layer. Here, the depth of the trench 10 can be adjusted in the range of about $0.5\mu\text{m} \sim 10\mu\text{m}$, in accordance with the desired value of the capacitance.

Figure 3C illustrates a process for forming a second opening and a fourth conductive layer 20 which functions as a first electrode of the capacitor. After forming the inter-planarizing layer 32, the second opening is formed to expose the source region 2 of the second memory cell M2. Thereafter, the fourth conductive layer 20 having a thickness of about $300\text{\AA} \sim 4000\text{\AA}$, which functions as the first electrode of the capacitor, e.g., an impurity-doped fourth polycrystalline silicon layer is deposited both on the surface of the second opening and on the inter-planarizing layer 32, so as to form the electrode pattern as shown in Figure 3C.

Figure 3D illustrates a process for removing the fourth insulating layer and the inter-planarizing layer, wherein, by using the nitride layer N as an etch blocking layer, the fourth insulating layer and the inter-planarizing layer, which are disposed between the second conductive layer 11 and the fourth conductive layer 20, are removed by wet

etching, thereby increasing the surface area of the first electrode pattern of each memory cell.

Figure 3E illustrates a process for forming a dielectric film 33 and a sixth conductive layer 34 serving as a second electrode of the capacitor. After the process shown in Figure 3D, the dielectric film 33 is simultaneously formed on both the second conductive layer 11 and the fourth conductive layer 20, and then, the sixth conductive layer 34 serving as the second electrode of the capacitor having a thickness of about $500\text{\AA} \sim 5000\text{\AA}$, e.g., an impurity-doped sixth polycrystalline silicon layer, is deposited, thereby completing the first memory cells M1 and M3 and the second memory cell M2. Here, the dielectric film 33 is of an oxide layer structure or an ONO structure such as HTO layer or LTO layer.

After performing the process illustrated in Figure 3E, the planarizing layer, e.g., BPSG layer is deposited to effect the planarizing, and then, metal electrodes are formed, thereby completing the DRAM having both the stack-trench capacitor cells and the stack capacitor cells.

As described in the above, the capacitor according to the present invention uses a combined stack-trench capacitor as the first capacitor of the conventional SSC structure, and uses a stack capacitor as the second capacitor of the conventional SSC structure. Accordingly, in manufacturing the combined stack-trench (or trench) capacitor, sufficient storage area of each capacitor can be obtained without being restricted by the distance between the second capacitors, i.e., the stack capacitors. In addition, during the formation of the second

capacitor (stack capacitor), the first capacitor, i.e., the combined stack-trench (trench) capacitor can markedly decrease the step coverage problem compared with the conventional first capacitor, i.e., stack capacitor, so that the processes are easily performed.

Furthermore, in a memory cell array in accordance with the present invention, because the first memory cells having combined stack-trench (or trench) capacitors and the second memory cells having the stack capacitors are arranged adjacent to one another both in the row and in the column direction, memory cells having the trench are alternately formed. As a result, it is advantageous in that the leakage current between memory cells with trench and the soft errors resulting from alpha particles can be removed.

Moreover, by etching the oxide layer and the interplanarizing layer disposed under the conductive layer serving as the first electrode in the capacitor of the second embodiment of the present invention described above, the areas of the upper portion, the side portion as well as the bottom portion of the conductive layer are utilized as the first electrode of the capacitor, so that the storage area of the capacitor can be maximized. Therefore, the decrease of the capacitance caused by the increase of the packing density of the highly integrated semiconductor memory device, can be improved by means of this structural approach.

CLAIMS:

1. A highly integrated semiconductor memory device comprising first and second pluralities of memory cells, each memory cell of said first plurality of memory cells including a first switching transistor formed on a semiconductor substrate and a first capacitor coupled to said first switching transistor, each memory cell of said second plurality of memory cells including a second switching transistor formed on said semiconductor substrate and a second capacitor coupled to said second switching transistor, and each of said first and second pluralities of memory cells being alternately disposed in each of a plurality of rows,

wherein each said first capacitor comprises a first storage electrode including a trench portion formed partially in said substrate and a first stack portion, and said first stack portion has overlap portions each extended to overlap a portion of adjacent second memory cells, and

wherein each said second capacitor comprises a second storage electrode including only a second stack portion and thus not including a trench portion partially formed in said substrate, wherein said second stack portion has a contact portion and also has overlap portions, each overlap portion extending to overlap an overlap portion of said first stack portion of adjacent first memory cells.

2. A highly integrated semiconductor memory device as claimed in claim 1, wherein said first memory cells and said second memory cells are disposed alternately and adjacent one



another in both row and column direction.

3. A highly integrated semiconductor memory device as claimed in claim 1 or 2, wherein the trench portion of said first capacitor is an outside trench capacitor.

4. A highly integrated semiconductor memory device as claimed in any preceding claim, wherein the depth of the trench is in the range of about $0.5\mu\text{m}$ ~ $10\mu\text{m}$.

5. A highly integrated semiconductor memory substantially as herein described with reference to Figures 1, 2 or 3E of the accompanying drawings.

6. A method for manufacturing a highly integrated semiconductor memory device comprising in the recited order the steps of:

defining active regions by growing field oxide layers on a first conductivity type semiconductor substrate;

forming transistors, which are elements of a memory cell, on said active regions, and forming a first insulating layer over the resultant structure;

forming bit lines so as to be connected to respective drain regions of said transistors, and forming a second insulating layer over the resultant structure;

forming first openings by exposing predetermined portions of the source regions so as to form first memory cells having a capacitor with a trench portion and a first stack



portion;

forming trenches in the semiconductor substrate by using said first openings;

forming capacitors both on the surface of said trenches and on said second insulating layer, and forming a third insulating layer on the resultant structure;

forming second openings in order to expose source regions of the transistors disposed adjacent said first memory cells in both row and column directions; and

forming capacitors with second stack portions through said second openings.

7. A method for manufacturing a highly integrated semiconductor memory device as claimed in claim 6, wherein said step for forming capacitors with second stack portions consists of forming a conductive layer serving as a first electrode of a stack capacitor through the second opening.

8. A method for manufacturing a highly integrated semiconductor memory device as claimed in claim 6 or 7, wherein said steps for forming the second insulating layer includes the step of forming a first oxide layer, a nitride layer and a second oxide layer, successively, after forming said bit lines.

9. A method for manufacturing a highly integrated semiconductor memory device as claimed in claim 8, wherein said first oxide layer and said second oxide layer are HTO layer.



10. A method for manufacturing a highly integrated semiconductor memory device as claimed in any of claims 6 to 9, wherein said step for forming capacitors and third insulating layer consists of forming a conductive layer, serving as a first electrode of a capacitor, both on the surface of said trench and on said second oxide layer, and then depositing an inter-planarizing layer on the resultant structure.

11. A method for manufacturing a highly integrated semiconductor memory device as claimed in claim 10, wherein said inter-planarizing layer is a SOG layer.

12. A method for manufacturing a highly integrated semiconductor memory device as claimed in claim 10, wherein said inter-planarizing layer is a stacked layer formed by SOG layer and HTO layer.

13. A method for manufacturing a highly integrated semiconductor memory device as claimed in claim 10, wherein said inter-planarizing layer is a stacked layer formed by HTO layer and BPSG layer.

14. A method for manufacturing a highly integrated semiconductor memory device as claimed in any of claims 10 to 13, wherein, after said step of forming capacitors and third insulating layers, said second oxide layer and said inter-planarizing layer formed on said nitride layer are removed.



15. A method for manufacturing a highly integrated semiconductor memory device as claimed in claim 14, wherein said second oxide layer and said inter-planarizing layer are removed by wet etching method.

16. A method for manufacturing a highly integrated semiconductor memory device as claimed in claim 14 or 15, wherein, after the step of etching said oxide layer and said interplanarizing layer, dielectric films are simultaneously formed over the exposed entire surface of said conductive layers.

17. A method for manufacturing a highly integrated semiconductor memory device as claimed in claim 16, wherein said dielectric film is formed by the step of forming a first oxide layer over the surface of said exposed conductive layer, forming a nitride layer over said first oxide layer, and forming a second oxide layer over said nitride layer.

18. A method for manufacturing a highly integrated semiconductor memory device as claimed in any of claims 6 to 17, wherein said first, second, and third insulating layers are HTO layer.

19. A method for manufacturing a highly integrated semiconductor memory device as claimed in any of claims 6 to 17, wherein said third insulating layer is formed by depositing and then reflowing a BPSG layer having a thickness of about



500Å ~ 4000Å, after the step of forming the capacitor of the first memory cell.

20. A method for manufacturing a highly integrated semiconductor memory device substantially as herein described with reference to any of Figures 2A to 2G and 3A to 3E of the accompanying drawings.