

A SYNCHRONIZED SWITCH-MODE POWER SUPPLY

The invention relates to switch-mode power supplies.

According to the present invention, there is
5 provided a switch mode power supply, comprising:

a transformer having first and second windings;

first switching means coupled to said first
winding for storing energy in said transformer during a
first interval of a switching cycle;

10 second switching means coupled to said second
winding and operated in a flyback converter mode for
depleting said stored energy from said transformer during a
flyback interval of said switching cycle;

control means coupled to said transformer and
15 responsive to the depletion of said stored energy for
controlling the duty cycle of said first switching means;

a source of an input voltage;

means responsive to the cyclical switching of said
first switching means for generating an output voltage from
20 said input voltage; and

a negative feedback circuit responsive to said
output voltage for generating a control voltage that is
applied to said transformer during said flyback interval to
vary the rate of depletion of said stored energy, thereby
25 varying said duty cycle in a manner that regulates said
output voltage.

For a better understanding of the present invention, reference will now be made, by way of example to the accompanying drawings, in which:-

FIGURE 1 illustrates a power supply embodying an aspect of the invention;

FIGURES 2a-2d illustrate waveforms useful for explaining the run mode operation of the circuit of FIGURE 1 when loading varies;

FIGURES 3a-3g illustrate additional waveforms useful for explaining the run mode operation of the circuit of FIGURE 1 under a constant loading condition;

FIGURE 4 illustrates the construction of the isolation transformers that are used in the circuit of FIGURE 1;

FIGURES 5a-5d illustrate waveforms useful for explaining a standby operation of the power supply of FIGURE 1;

FIGURES 6a-6d illustrate transient waveforms useful for explaining the operation of the circuit of FIGURE 1 during start-up;

FIGURE 7 illustrates the circuit of FIGURE 1 that incorporates a modification to increase output power;

FIGURE 8 provides a table of performance data of the circuit of FIGURE 1 and also, for comparison purposes, of a conventional power supply; and

FIGURE 9 provides a table of additional performance data of the circuit of FIGURE 1 and also, for comparison purposes, of a conventional power supply.

FIGURE 1 illustrates a switch-mode power supply (SMPS) 200, embodying an aspect of the invention. SMPS 200 produces an output B+ supply voltage of +145 volts at terminal 99 that is used for energizing, for example, a deflection circuit 222 of a television receiver, not shown, and an output supply voltage V+ of +18 volts, that are both regulated. A mains supply voltage V_{AC} is rectified in a bridge rectifier 100 to produce an unregulated voltage V_{UR} at terminal 100a. A primary winding W_p of a flyback

isolation transformer T1 is coupled between terminal 100a and a drain electrode of a power chopper MOS field effect transistor (FET) Q1.

5 The source electrode of MOS transistor Q1 of
FIGURE 1 is coupled to a common conductor, referred to
herein as "hot" ground. The gate electrode of FET Q1 is
coupled via a coupling resistor 102 to a terminal 104 where
a pulse-width modulated signal V_5 is produced. Signal V_5
10 produces a switching operation in FET Q1. A secondary
winding W_3 of an isolation transformer T2, across which
signal V_5 is developed, is coupled between terminal 104 and
the hot ground conductor. A pair of back-to-back zener
diodes Z18A and Z18B provide gate protection for FET Q1.
Winding W_3 , winding W_p , FET Q1 and signal V_5 are at
15 potentials that are referenced to the hot ground conductor.

Transformers T1 and T2 are constructed in a manner
shown in FIGURE 4. Similar symbols and numerals in FIGURES
1 and 4 indicate similar items or functions.

20 FIGURES 3a-3g illustrate waveforms useful for
explaining the normal steady state operation or run mode of
the SMPS of FIGURE 1 under a constant loading condition.
Similar symbols and numerals in FIGURES 1 and 3a-3g
indicate similar items or functions.

During, for example, interval $t_0 - t_1$ of FIGURE 3b
25 of a corresponding given cycle or period, the voltage of
pulse signal V_5 is positive relative to the hot ground
conductor for maintaining FET Q1 of FIGURE 1 conductive
during interval $t_0 - t_1$ of FIGURE 3b. Consequently, a
current i_1 in winding W_p of FIGURE 1 is upramping, as shown
30 in FIGURE 3d, during interval $t_0 - t_1$. Therefore,
inductive energy is stored in transformer T1 of FIGURE 1.
At time t_1 of FIGURE 3d, FET Q1 of FIGURE 1 becomes
nonconductive.

35 After FET Q1 becomes nonconductive, the inductive
energy stored in winding W_p is transferred by flyback
transformer action to a secondary winding W_s of transformer
T1. Flyback pulses developed at corresponding terminals
108 and 109 of winding W_s are rectified by diodes

106 and 107, respectively, and filtered by capacitors 121 and 122, respectively, for producing DC voltages B+ and V+, respectively, that are all referenced to a second common conductor, referred to herein as "cold" ground. The cold
5 ground is conductively isolated from the hot ground conductor with respect to electrical shock hazard by transformers T1 and T2. FET Q1, transformer T1 and diodes 106 and 107 form an output stage of the SMPS.

A pulse-width modulator of SMPS 200 includes a
10 blocking oscillator 110, embodying an aspect of the invention, that produces switching signal V_5 for controlling the switching operation of FET Q1. Oscillator 110 includes a switching transistor Q2 having a base electrode that is also controlled or switched by signal V_5 .
15 Winding W_3 of transformer T2 provides positive feedback in oscillator 110 by developing signal V_5 . Transformer T2 has a primary winding W_1 that is coupled between voltage V_{UR} and the collector of transistor Q2 such that winding W_1 is referenced to the hot ground conductor. A secondary
20 winding W_2 of transformer T2 that is referenced to the cold ground conductor is conductively coupled to a diode D3 of a control circuit 120, embodying another aspect of the invention, that is also referenced to the cold ground conductor.

25 The cathode of diode D3 is coupled to the cold ground conductor via a capacitor C4. As explained later on, a DC control voltage V_4 , developed across capacitor C4, varies the nonconduction time, and therefore the duty cycle of transistor Q2 during each period.

30 A capacitor C2 is coupled between the base electrode of transistor Q2 and a terminal 104a. A resistor R2 is coupled between terminal 104a and terminal 104 where signal V_5 is developed. During interval $t_0 - t_1$ of FIGURE 3b, a current i_5 of FIGURE 3c is produced in resistor R2 of
35 FIGURE 1 that is coupled between terminals 104 and 104a. Current i_5 of FIGURE 3c, that is produced by signal V_5 of FIGURE 3b, charges capacitor C2 of FIGURE 1 in a manner

that turns on transistor Q2, during interval $t_0 - t_1$ of FIGURE 3d.

During normal operation, when transistor Q2 of FIGURE 1 is conductive, a current i_2 of FIGURE 3d in winding W_1 of FIGURE 1 increases linearly, until the emitter voltage of transistor Q2, that is developed across an emitter resistor R4, is sufficiently high to initiate a rapid turn-off operation of transistor Q2. Feedback resistor R4 is coupled between the emitter of transistor Q2 and the hot ground conductor. Resistor R4 causes a gradual decrease of current i_5 of FIGURE 3c when transistor Q2 of FIGURE 1 is conductive until transistor Q2 ceases to conduct at time t_1 of FIGURE 3c. Resistor R4 of FIGURE 1 also serves to optimize the switching condition and to provide current protection for transistor Q2. The result is that the voltage across winding W_1 reverses polarity. The turn-off operation is rapid because of the positive feedback caused by winding W_3 in developing signal V_5 .

As indicated before, winding W_3 provides pulse drive signal V_5 that controls also FET Q1. The conduction interval in each cycle of FET Q1 and transistor Q2 remains substantially constant or unaffected by loading. Therefore, advantageously, the stored energy in transformer T1, when transistor Q1 becomes nonconductive, is substantially constant for a given level of voltage V_{UR} . However, the conduction interval may vary when a variation in voltage V_{UR} occurs.

When transistor Q2 ceases to conduct, a downramping current i_4 of FIGURE 3e is produced in winding W_2 of transformer T2 of FIGURE 1. Current i_4 causes diode D3 of FIGURE 1 to be conductive, and charges capacitor C4, during interval $t_1 - t_4$ of FIGURE 3e. For a given level of voltage V_{UR} of FIGURE 1, and for a given duty cycle of transistor Q2, the charge added to capacitor C4 is the same in each cycle. During interval $t_1 - t_4$, control voltage V_4 of FIGURE 1, except for the forward voltage drop in diode D3, is substantially developed across winding W_2 .

In accordance with an aspect of the invention, voltage V_4 determines the length of interval $t_1 - t_4$ of FIGURE 3e that is required to deplete the magnetic energy stored in transformer T2 of FIGURE 1. When, at time t_4 , of FIGURE 3e, current i_4 becomes zero, the polarity of signal V_5 of FIGURE 3b changes as a result of resonance oscillations in the windings of transformer T2. Therefore, positive current i_5 of FIGURE 3c is generated. As explained before, when current i_5 is positive, it causes transistors Q1 and Q2 to be conductive.

During the aforementioned nonconduction interval $t_1 - t_4$ of FIGURE 3b of transistors Q1 and Q2 of FIGURE 1, signal V_5 is negative, as shown during interval $t_1 - t_4$ of FIGURE 3b. Consequently, a current in the opposite polarity, as shown in FIGURE 3c, flows through capacitor C2 of FIGURE 1, during interval $t_1 - t_2$ of FIGURE 3c and through diode D1 during interval $t_2 - t_4$ of FIGURE 3c. The resulting charge in capacitor C2 produces a voltage in capacitor C2 in such a polarity that tends to turn on transistor Q2 rapidly, when, at time t_4 of FIGURES 3b, signal V_5 reverses polarity.

Control circuit 120 of FIGURE 1, that is referenced to the cold ground conductor, controls the duty cycle of oscillator 110 by varying control voltage V_4 across capacitor C4. A transistor Q4 of circuit 120 is coupled in a common base amplifier configuration. The base voltage of transistor Q4 is obtained via a temperature compensating forward biased diode D5 from a +12V voltage regulator VR1. Regulator VR1 is energized by voltage $V+$.

A resistor R51 is coupled between the emitter of transistor Q4 and terminal 99. As a result of the common base operation, a current i_8 in resistor R51 is proportional to voltage $B+$. An adjustable resistor R5, that is used for adjusting the level of voltage $B+$, is coupled between the cold ground conductor and a junction terminal between the emitter of transistor Q4 and resistor R51. Resistor R51 is used for controlling the level of the current in transistor Q4. Thus, an adjustable preset

portion of current i_8 flows to the cold ground conductor through resistor R5, and an error component of current i_8 flows through the emitter of transistor Q4.

5 The collector current of transistor Q4 is coupled to the base of a transistor Q3 for controlling a collector current of transistor Q3. The collector of transistor Q3, forming a high output impedance, is coupled to the junction between capacitor C4 and diode D3. When transistor Q2 becomes nonconductive the stored energy in transformer T2
10 causes current i_4 to flow via diode D3 into capacitor C4, as indicated before. Regulation of the power supply is obtained by controlling control voltage V_4 . Voltage V_4 is controlled by controlling the loading across winding W_2 of transformer T2 by means of transistor Q3.

15 The collector current of transistor Q3, that forms a current source having a high output impedance, is coupled to capacitor C4 that operates as a flywheel. In steady state, the amount of charge that is added to capacitor C4 during interval $t_1 - t_4$ of FIGURE 3e is equal to the amount
20 of charge that is removed by transistor Q3 from capacitor C4 in a given period $t_0 - t_4$.

FIGURES 2a-2d illustrate waveforms useful for explaining the regulation operation of the SMPS of FIGURE 1 under different loading conditions. Similar symbols and
25 numerals in FIGURES 1, 2a-2d and 3a-3g indicate similar items or functions.

After, for example, time t_A of FIGURES 2a-2d, the power supply current loading across capacitor 121 of FIGURE 1 decreases and voltage B+ tends to increase. As a result
30 of the increase in voltage B+, transistor Q3 conducts a higher level of collector current. Therefore, voltage V_4 of FIGURE 2c across capacitor C4 of FIGURE 1 becomes smaller. Therefore, a longer time is required in each period for depleting the stored inductive energy from transformer T2
35 of blocking oscillator 110, after transistor Q2 becomes nonconductive. It follows that the length of the interval, $t_A - t_B$, of FIGURE 2a, in a given cycle, when transistor Q2 of oscillator 110 of FIGURE 1 is nonconductive, increases

under reduced loading condition. The result is that the duty cycle, that is the ratio between the "on" time to the "off" time of transistor Q1 decreases, as required for proper regulation.

5 In steady state, voltage V_4 is stabilized at a level that causes an equilibrium between the charging and discharging currents of capacitor C4. The increase in voltage B+ is capable of causing, advantageously, a proportionally greater change in voltage V_4 , as a result of
10 amplification and current integration of the collector current of transistor Q3 in capacitor C4. In a transient condition, as long as voltage B+ is, for example, greater than +145 volts, voltage V_4 will decrease.

The result is that voltage V_4 of FIGURE 1 tends to
15 change in a manner that tends to nullify the aforementioned tendency of voltage B+ to increase under reduced loading. Thus, regulation is obtained in a negative feedback manner. In the extreme case, a short circuit across winding W_2 could inhibit oscillation in oscillator 110 thus providing,
20 advantageously, an inherent fail safe feature, as described later on.

Conversely, a tendency of voltage B+ to decrease will increase the duty cycle of transistors Q1 and Q2 in a manner that provides regulation. Thus, the nonconduction
25 interval of transistor Q1 varies with current loading at a terminal 99 where voltage B+ is developed.

Processing voltage B+ for producing control voltage V_4 is accomplished, advantageously, in a DC coupled signal path for improving error sensing. Also, a change in
30 voltage B+ is capable of causing a proportionally greater change in voltage V_4 thus improving error sensitivity. Only after the error in voltage B+ is amplified, the amplified error contained in DC coupled voltage V_4 is transformer or AC coupled to effectuate pulse-width
35 modulation. The combination of such features improves the regulation of voltage B+.

Another way by which an arrangement similar to control circuit 120 is used for regulation purposes is

shown and explained in a copending patent application GB-A-2230659 (U.S. Patent Application 424,353, filed 19 October 1989, entitled A SYNCHRONIZED SWITCH-MODE POWER SUPPLY, RCA 85439). There, a voltage that is produced
5 similarly to voltage V_4 of FIGURE 1 is transformer coupled to a sawtooth generator. The transformer coupled voltage varies a sawtooth signal that is used for producing a pulse-width modulated control signal.

10 A zener diode D4 is coupled in series with a resistor R_{D4} , between the base and collector electrodes of transistor Q3. Zener diode D4, advantageously, limits voltage V_4 to about 39 volts.

In accordance with a feature of the invention, zener diode D4 limits the frequency of oscillator 110, or
15 the minimum cut-off time of transistors Q2 and Q1. In this way, the maximum power transferred to the load is, advantageously, limited for providing over-current protection.

For safe operation, it may be desirable to have
20 secondary current i_3 in winding W_s decay to zero before transistor Q1 is turned on again. This means that the decay time of current i_3 should be, preferably, shorter than the minimum decay time of current i_4 of blocking oscillator 110. This condition can be met by a proper
25 choice of the primary inductance of transformer T2 and the value of zener diode D4.

Standby operation is initiated by operating SMPS
200 in a low power operation mode. The low power operation mode occurs when the power demand from the SMPS drops below
30 20-30 watts. For example, when a horizontal oscillator, not shown, that is controlled by a remote control unit 333, ceases operating, horizontal deflection circuit 222, that is energized by voltage B+ ceases operation as well. Therefore, the loading at terminal 99, where voltage B+ is
35 produced, is reduced. Consequently, voltage B+ and the error current in transistor Q4 tend to increase. Therefore, transistor Q3 saturates, causing a near short circuit across winding W_2 of transformer T2, that causes

voltage V_4 to be approximately zero. Consequently, unlike in the run-mode of operation, a positive pulse of signal V_5 cannot be generated by resonance oscillations in transformer T2. It follows that the regenerative feedback loop is prevented from initiating the turn on of transistor Q2. Consequently, continuous oscillations cannot be sustained.

However, transistor Q2 is periodically triggered into switching in a burst mode operation by an upramping portion of a half wave rectified voltage of a signal V_7 . Signal V_7 occurs at the mains frequency, such as 50Hz. Signal V_7 is derived from bridge rectifier 100 and is applied to the base of transistor Q2 via a series arrangement of a resistor R1 and a capacitor C1. The series arrangement operates as a differentiator that produces a current i_7 .

FIGURES 5a-5d illustrate waveform during standby operation, indicating that burst mode switching operation of oscillator 110 occurs during an interval t_{10} - t_{12} followed by a dead time interval t_{12} - t_{13} , when no trigger pulses of signal V_5 are present in the blocking oscillator. Similar symbols and numerals in FIGURES 1 and 5a-5d indicate similar items or functions.

A parallel arrangement of a capacitor C3 of FIGURE 1 and a resistor R3 is coupled in series with a diode D2 to form an arrangement that is coupled between the hot ground conductor and junction terminal 104a, between capacitor C2 and resistor R2. A diode D1 is coupled in parallel with capacitor C2.

During normal run mode operation, capacitor C3 remains charged to a constant voltage V_6 by the positive voltage pulses of signal V_5 that is developed in winding W_3 each time transistor Q2 is conductive. Therefore, during normal run mode operation, capacitor C3 has no effect.

During standby operation, capacitor C3 discharges during the long inactive periods or dead time, as shown between times t_{12} - t_{13} in FIGURE 5b.

Immediately after time t_{10} of FIGURE 5a of a given interval t_{10} - t_{13} , current i_7 of FIGURE 1 that is produced by voltage differentiation in capacitor C1 increases from zero to a maximum positive value. As a result, a base current, produced in transistor Q2, causes transistor Q2 to be conductive. When transistor Q2 becomes conductive, a positive pulse of signal V_5 is produced in winding W_3 that renders transistors Q1 and Q2 conductive.

Similarly to normal run mode operation that was described before, transistor Q2 remains conductive until the magnitude of the base current of transistor Q2 is insufficient to maintain transistor Q2 in saturation, as collector current i_2 is upramping. Then, collector voltage V_2 increases and signal V_5 decreases. The result is that transistor Q2 is turned-off.

The voltage across capacitor C2 produces negative current i_5 that discharges capacitor C2 via a diode D7 and that maintains transistor Q2 in cut-off. As long as a magnitude of negative current i_5 is larger than that of positive current i_7 , the base current in transistor Q2 is zero and transistor Q2 remains nonconductive. When the magnitude of negative current i_5 of FIGURE 1 becomes smaller than current i_7 , transistor Q2 is turned on again and positive current i_5 is generated.

During a substantial portion of a given conduction interval of transistor Q2, current i_5 flows entirely via capacitor C2 to form the base current of transistor Q2. Because collector current i_2 is upramping, the emitter voltage of transistor Q2 increases in an upramping manner, causing the voltage at the anode of diode D2 to increase. When the voltage at the anode of diode D2 becomes sufficiently positive, diode D2 begins conducting. Therefore, a substantial portion of current i_5 is diverted by capacitor C3 from the base of transistor Q2. The result is that the base current becomes insufficient to sustain the collector current of transistor Q2. Therefore, the positive feedback signal path causes transistor Q2 to turn-

off. Thus, the peak amplitude of current i_2 is determined by the level of voltage V_6 across capacitor C3.

During interval $t_{10} - t_{12}$ of FIGURES 5a-5d, capacitor C3 of FIGURE 1 is charged by positive current i_5 . Therefore, voltage V_6 of FIGURE 5b becomes progressively larger. Voltage V_6 that becomes progressively larger causes the conduction interval during each cycle that occurs in interval t_{10} - t_{12} of FIGURES 5a-5d to become progressively longer.

During a corresponding nonconduction portion of each cycle that occurs in interval t_{10} - t_{12} , capacitor C2 of FIGURE 1 is discharged. The length of the nonconduction interval of transistor Q2 in each cycle is determined by the time required for discharging capacitor C2 to such a level that causes a magnitude of negative current i_5 to be smaller than that of positive current i_7 . That nonconduction interval becomes progressively longer because capacitor C2 is charged to a progressively higher voltage and also because the magnitude of current i_7 becomes progressively smaller. Therefore, positive base current will begin flowing in the base of transistor Q2 after progressively longer nonconduction intervals.

At time t_{12} of FIGURE 5a current i_7 is zero. Therefore, burst mode operation that occurred during interval t_{10} - t_{12} cannot continue and the long dead time interval t_{12} - t_{13} occurs in which no switching operation happens. At time t_{13} , positive current i_7 is generated again and a subsequent burst mode switching interval occurs in transistors Q1 and Q2.

During the burst mode interval t_{10} - t_{12} of FIGURE 5d, the length of the conduction interval in each cycle increases progressively, as explained before. Such operation may be referred to by the term soft start operation. Because of the soft start operation, capacitor 121 for example, of SMPS 200 is charged or discharged gradually. Voltage V_6 by being lower than during run mode operation maintains the switching frequency of transistors Q1 and Q2 of FIGURE 1 above the audible range in SMPS 200

of FIGURE 1 throughout interval t_{10} - t_{12} of FIGURE 5a. As a result of the soft start operation and of the high switching frequency during standby, noise produced by parasitic mechanical vibration in inductors and

5 transformers of SMPS 200 of FIGURE 1 is, advantageously, substantially reduced.

The burst mode operation during interval t_{10} - t_{12} of FIGURE 5c produces voltage V_+ of FIGURE 1 at a sufficient level to enable the operation of remote control
10 unit 333 of FIGURE 1, during standby. Because of the burst mode operation, the energy consumed in SMPS 200 is maintained substantially lower, at about 6 watts, than during normal run mode operation.

To generate voltage V_+ at the required level for
15 operating remote control unit 333, a corresponding average duty cycle of transistors Q1 and Q2 that is substantially lower than during run mode is required. The length of the conduction interval in transistor Q1, for example, should be longer than the storage time of transistor Q1.

20 Accordingly, by operating in the burst mode, the conduction interval of transistor Q1 in each cycle can be maintained longer for obtaining the required lower average duty cycle than if continuous switching operation had occurred during standby. Such continuous switching operation in
25 transistors Q1 and Q2 occurs during normal run mode operation when no dead time intervals such as interval t_{12} - t_{13} of FIGURE 5d occur.

The SMPS has also a soft start-up feature, as will now be explained with the aid of waveforms in FIGURES 6a-
30 6d. Similar symbols and numerals in FIGURES 1, 5a-5d and 6a-6d indicate similar items or functions. The start-up mode is similar to the stand-by operation. When the power supply is first turned on, capacitors C3 and C4 are discharged and there is no forward bias on the base of
35 transistor Q2. Oscillation is initiated by feeding a small portion of rectified AC supply signal V_7 to the base of transistor Q2. As illustrated by FIGURE 6d, the oscillator duty cycle is initially very short, or the interval in each

cycle when transistor Q2 is nonconductive is long, because winding W2 of transformer T2 is heavily loaded by the discharged capacitor C4. The charge on capacitors C3 and C4, and voltage B+ build up gradually over a period of about 15msec, as shown in FIGURE 6c. Normal operation begins following this slow build up.

In case of a short circuit at terminal 99 of FIGURE 1, for example, SMPS 200 goes into an intermittent mode operation, in a similar manner to the stand-by operation mode. For example, if capacitor C121 of FIGURE 1 is short circuited, the increase in current i_3 flowing through secondary winding W_s of transformer T1 causes a higher negative bias to develop across a resistor R6 that is coupled to the emitter of transistor Q3. Base current then flows into transistor Q3 through a diode D55, causing transistor Q3 to saturate and to clamp its collector voltage V4 to ground. The consequent loading of transformer T2 causes SMPS 200 to operate in the intermittent burst mode as described for stand-by mode operation.

The low voltage supply portion of SMPS 200 that produces voltage V+ may be arranged to operate as a forward converter in case of, for example, high audio power requirements. FIGURE 7 shows a modification of the circuit of FIGURE 1 for obtaining forward converter operation. A resistor Rx and a diode Dy of FIGURE 7 serve as an overload protection, as explained later on. Similar symbols and numerals in FIGURES 1 and 7 indicate similar items or functions. Should an overload occur when the modification shown in FIGURE 7 is employed to provide the high power audio supply, resistor Rx senses the excess current and provides negative bias to the emitter of transistor Q3.

FIGURE 8 shows, in a table form, the variation of voltage B+ caused by a corresponding variation in a beam current flowing in an ultor electrode, not shown, of a television receiver. Voltage B+ energizes the deflection circuit output stage, not shown, for producing the ultor voltage and the beam current. FIGURE 9 shows, in a table

form, a variation of voltage B+ caused by a variation of mains supply voltage V_{AC} .

For comparison purposes, row No. 1 in each of the tables of FIGURES 8 and 9 provides data obtained when a conventional prior art SMPS using an integrated circuit TDA4601 control circuit and a power transformer Orega No. V4937700 is utilized. Row No. 2 in each of the tables of FIGURES 8 and 9 provides data obtained when the unmodified SMPS of FIGURE 1 is utilized. As can be seen, the performance of SMPS 200 of FIGURE 1 is superior.

Reference is invited to copending patent application GB 9004975.0 from which this application is derived.



RCA 85438 DIV A

CLAIM :

1. A switch mode power supply, comprising:
a transformer having first and second windings;
first switching means coupled to said first winding for storing energy in said transformer during a first interval of a switching cycle;
second switching means coupled to said second winding and operated in a flyback converter mode for depleting said stored energy from said transformer during a flyback interval of said switching cycle;
control means coupled to said transformer and responsive to the depletion of said stored energy for controlling the duty cycle of said first switching means;
a source of an input voltage;
means responsive to the cyclical switching of said first switching means for generating an output voltage from said input voltage; and
a negative feedback circuit responsive to said output voltage for generating a control voltage that is applied to said transformer during said flyback interval to vary the rate of depletion of said stored energy, thereby varying said duty cycle in a manner that regulates said output voltage.
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