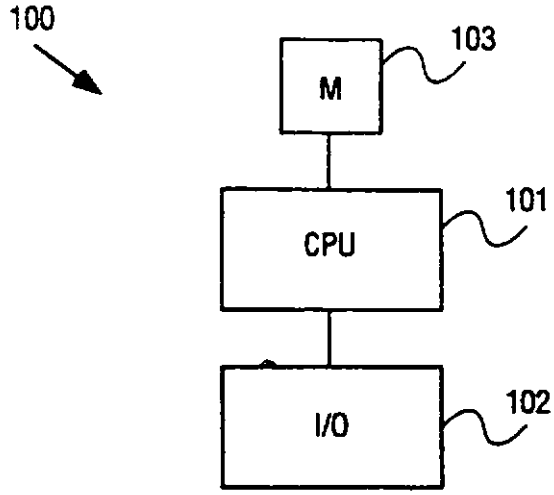

100
M
103
CPU
101
I/O
102

FIG. 1

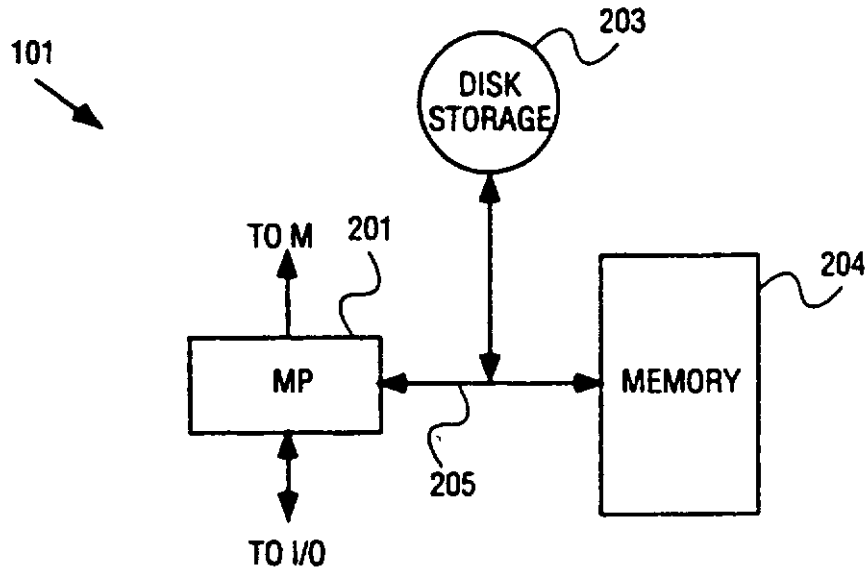

101
DISK STORAGE
203
TO M
201
MP
MEMORY
204
205
TO I/O

FIG. 2

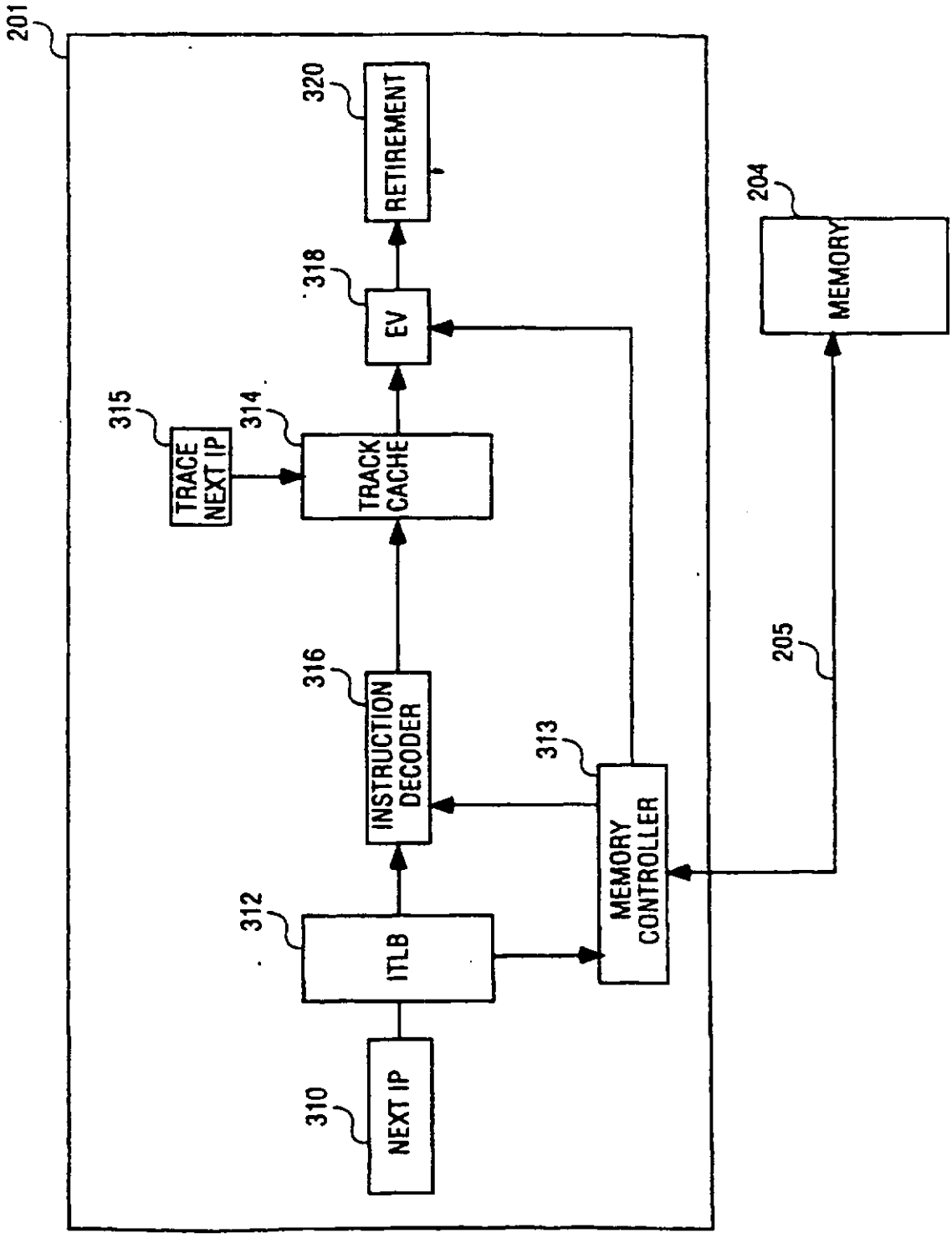

201
320
RETIREMENT
204
MEMORY
318
EV
315
TRACE NEXT IP
314
TRACK CACHE
316
INSTRUCTION DECODER
313
MEMORY CONTROLLER
205
312
ITLB
310
NEXT IP

FIG. 3

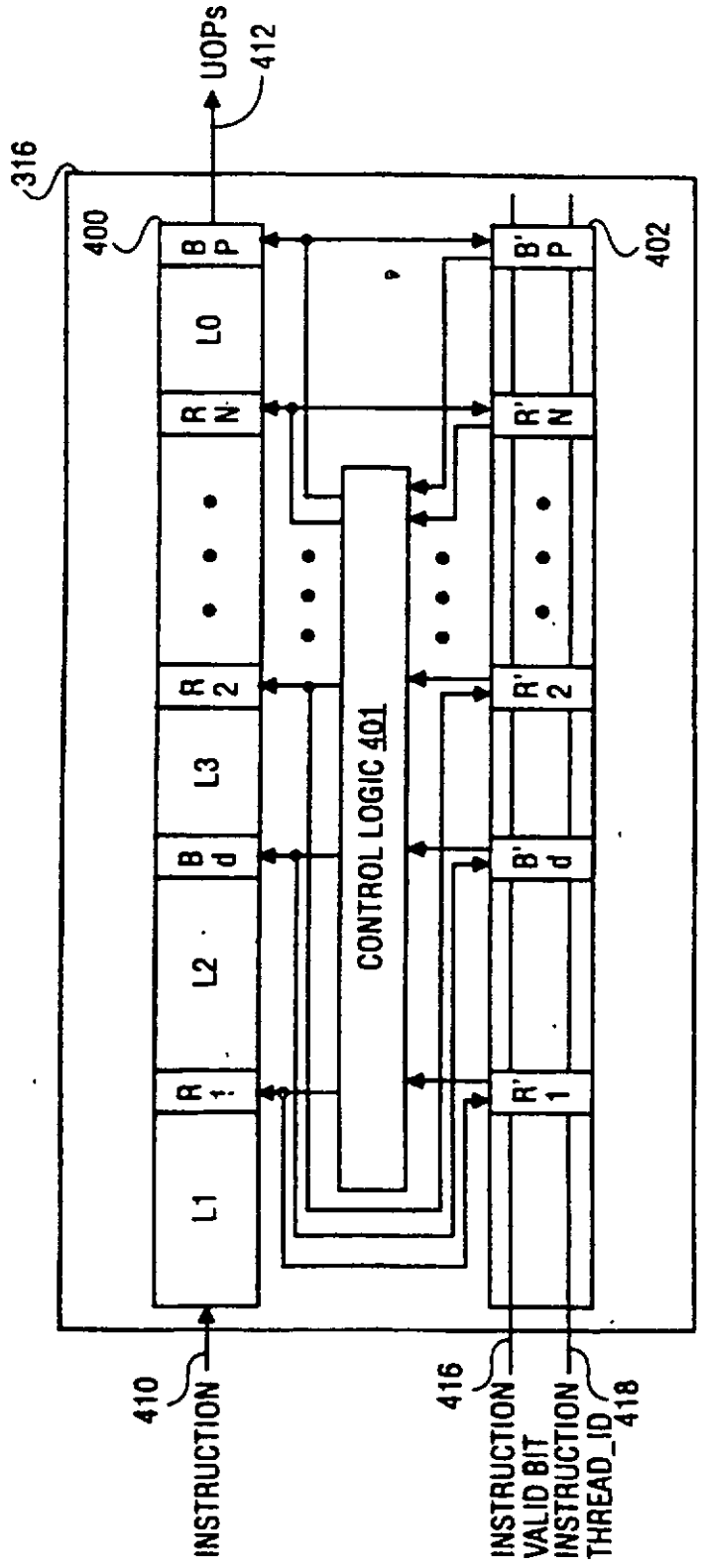

UOPs
412
316
400
402
BP
L0
RN
R2
L3
Bd
L2
R1
L1
CONTROL LOGIC 401
B'P
R'N
R'2
B'd
R'1
410
INSTRUCTION
416
INSTRUCTION VALID BIT
INSTRUCTION THREAD_ID
418

FIG. 4

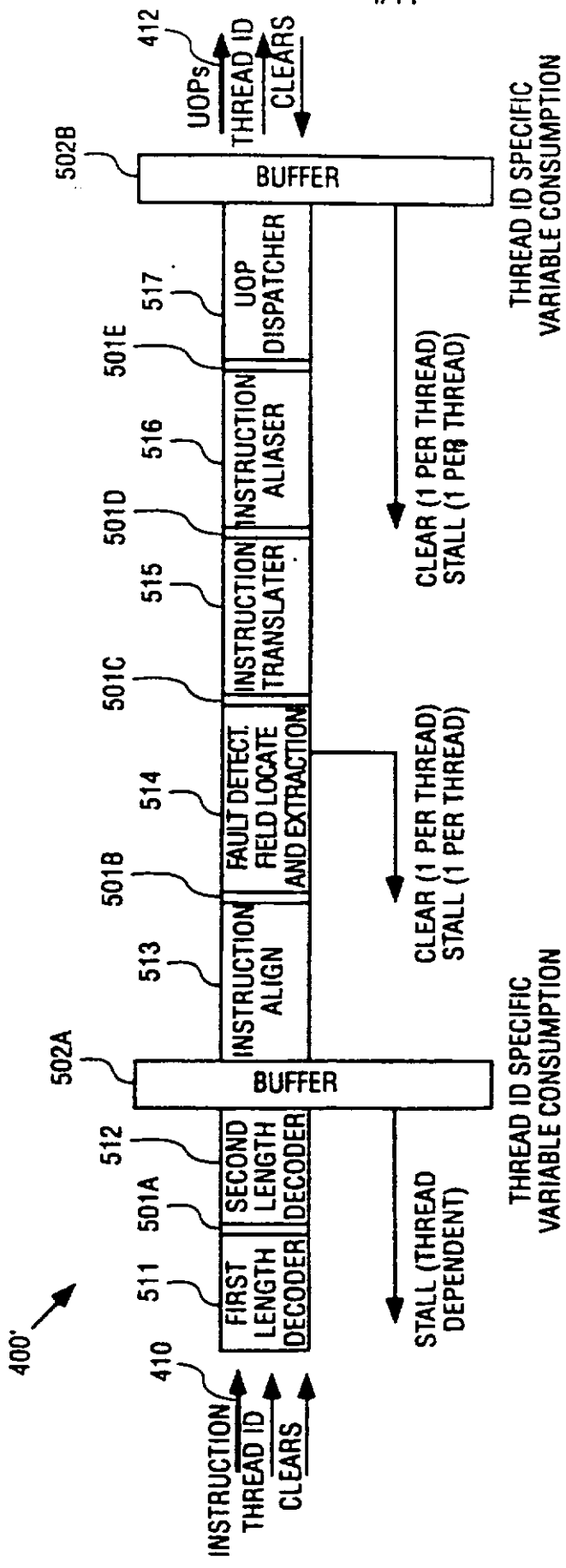

400'
INSTRUCTION
THREAD ID
CLEARS
410
FIRST LENGTH DECODER
511
SECOND LENGTH DECODER
501A
512
BUFFER
502A
INSTRUCTION ALIGN
513
FAULT DETECT. FIELD LOCATE AND EXTRACTION
501B
514
INSTRUCTION TRANSLATER
501C
515
INSTRUCTION ALIASER
501D
516
UOP DISPATCHER
501E
517
BUFFER
502B
UOPs
THREAD ID
CLEARS
412
STALL (THREAD DEPENDENT)
THREAD ID SPECIFIC VARIABLE CONSUMPTION
CLEAR (1 PER THREAD) STALL (1 PER THREAD)
CLEAR (1 PER THREAD) STALL (1 PER THREAD)
THREAD ID SPECIFIC VARIABLE CONSUMPTION

FIG. 5

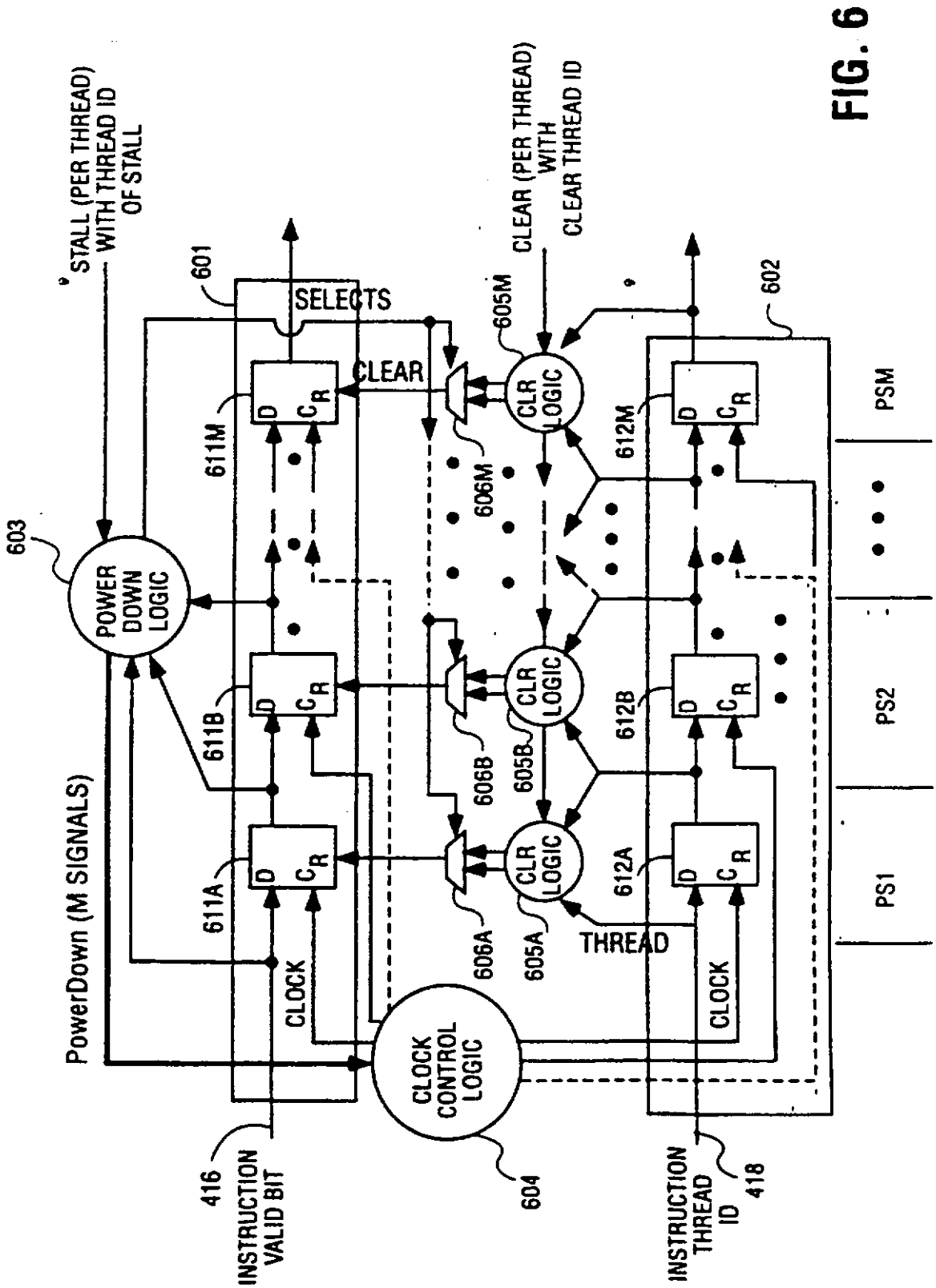

STALL (PER THREAD) WITH THREAD ID OF STALL
CLEAR (PER THREAD) WITH CLEAR THREAD ID
601
602
SELECTS
CLEAR
603
POWER DOWN LOGIC
611M
611B
611A
605M
606M
606B
605B
606A
605A
612M
612B
612A
CLR LOGIC
PSM
PS2
PS1
PowerDown (M SIGNALS)
CLOCK
THREAD
CLOCK CONTROL LOGIC
604
416
INSTRUCTION VALID BIT
INSTRUCTION THREAD ID
418

FIG. 6

Stall for NEXT TO LAST Pipestage (NLP)
$Stall_{(NLP)}$ = Valid Instruction in $Pipe_{(NLP)}$ AND ($ThreadID_{(NLP)}$= ThreadId of stall)

Stall for any other PipeStage X
$Stall_{(X)}$ = Valid Instruction in $Pipe_{(X)}$ AND Valid Instruction in $Pipe_{(X+1)}$ AND $Stall_{(NLP)}$

Powerdown for any PipeStage X
$Powerdown_{(X)}$ = NOT Valid Instruction in $Pipe_{(X-1)}$

Clock Enable for any PipeStage X
$Clock_{(X)}$ = NOT $Stall_{(X)}$ AND NOT $Powerdown_{(X)}$

Clear for any PipeStage X
$Clear_{(X)}$= $Clock_{(X)}$ AND [($ClearThread_{(Id0)}$ AND ($ThreadId_{(X-1)}$ = Id0)) OR ($ClearThread_{(Id1)}$ AND ($ThreadId_{(X-1)}$ = Id1))]
OR
Not $Clock_{(X)}$ AND [($ClearThread_{(Id0)}$ AND ($ThreadId_{(X)}$ = Id0)) OR ($ClearThread_{(Id1)}$ AND ($ThreadId_{(X)}$ = Id1))]

$ClearThread_{(Id0)}$ = There was a Clear on Thread Identification 0
$ClearThread_{(Id1)}$ = There was a Clear on Thread Identification 1
$Pipe_{(X)}$ = Any pipestage in the decode
$Pipe_{(X-1)}$ = Pipestage before Pipe(X)
$Pipe_{(X+1)}$ = Pipestage after Pipe(X)

FIG. 7

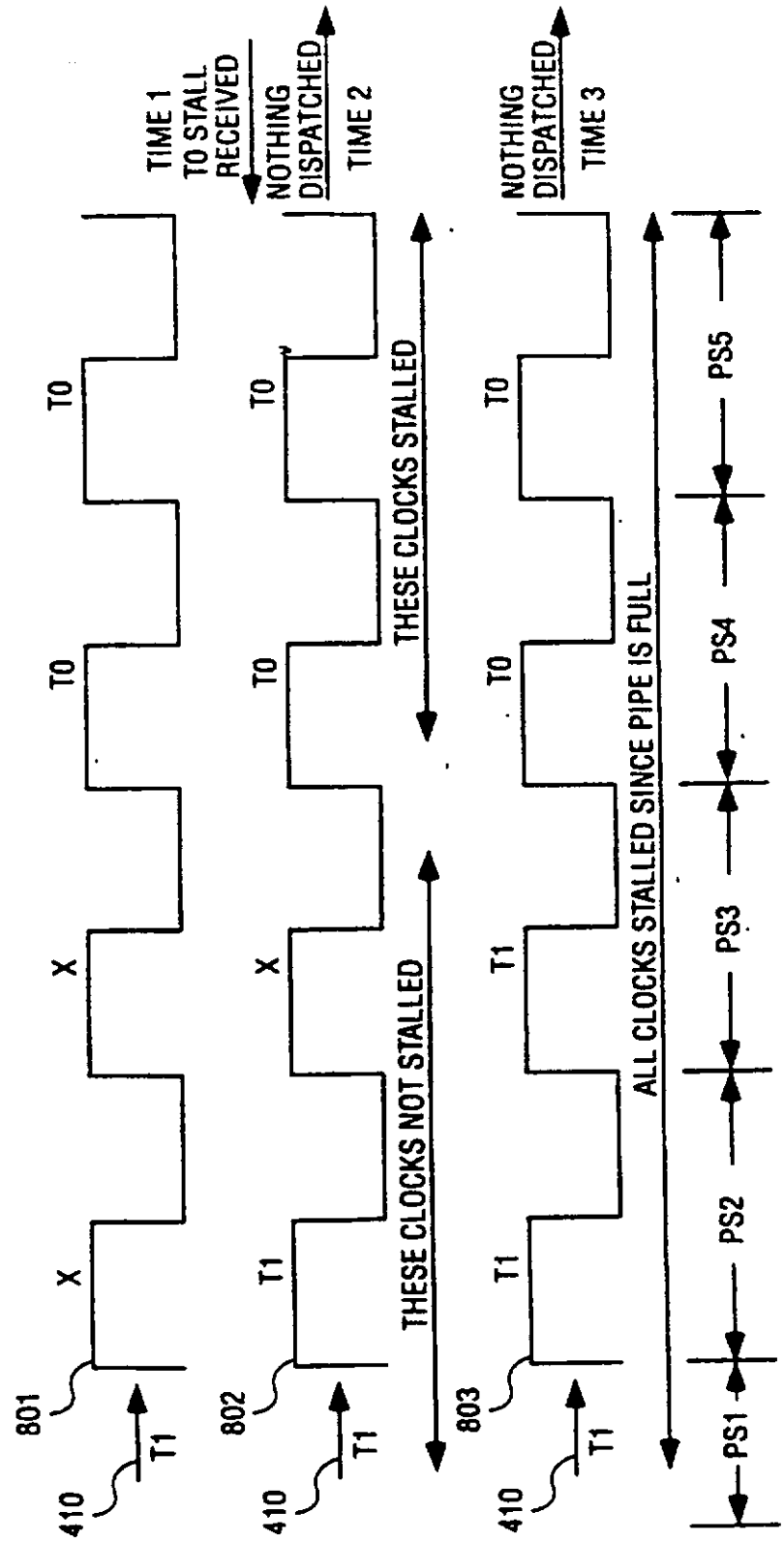

TIME 1
TO STALL RECEIVED
NOTHING DISPATCHED
TIME 2
NOTHING DISPATCHED
TIME 3
THESE CLOCKS STALLED
THESE CLOCKS NOT STALLED
ALL CLOCKS STALLED SINCE PIPE IS FULL
801
802
803
410
T1
X
T0
PS1
PS2
PS3
PS4
PS5

FIG. 8

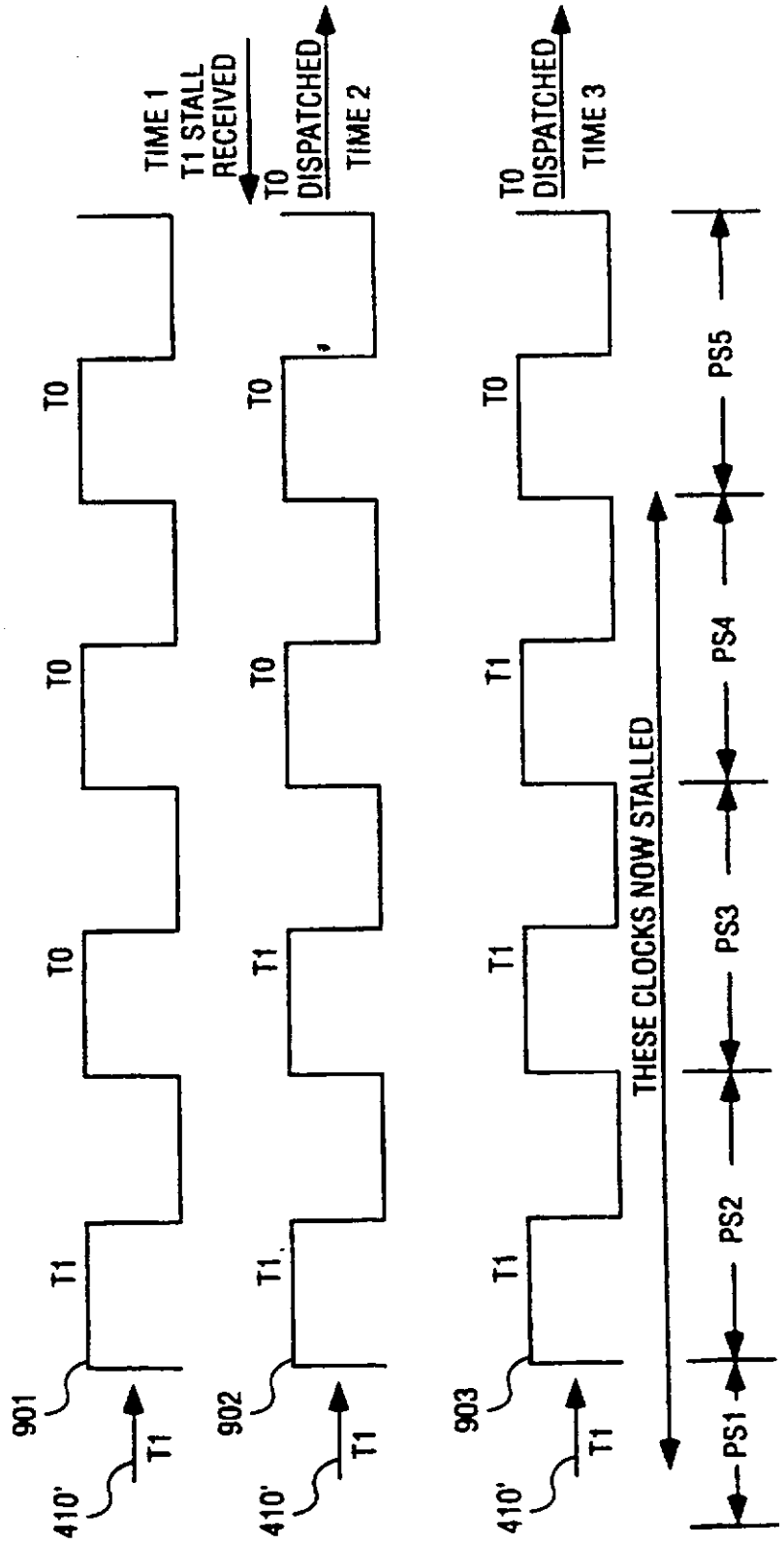

TIME 1
T1 STALL RECEIVED
T0 DISPATCHED
TIME 2
T0 DISPATCHED
TIME 3
T0
T1
901
902
903
410'
THESE CLOCKS NOW STALLED
PS1
PS2
PS3
PS4
PS5

FIG. 9

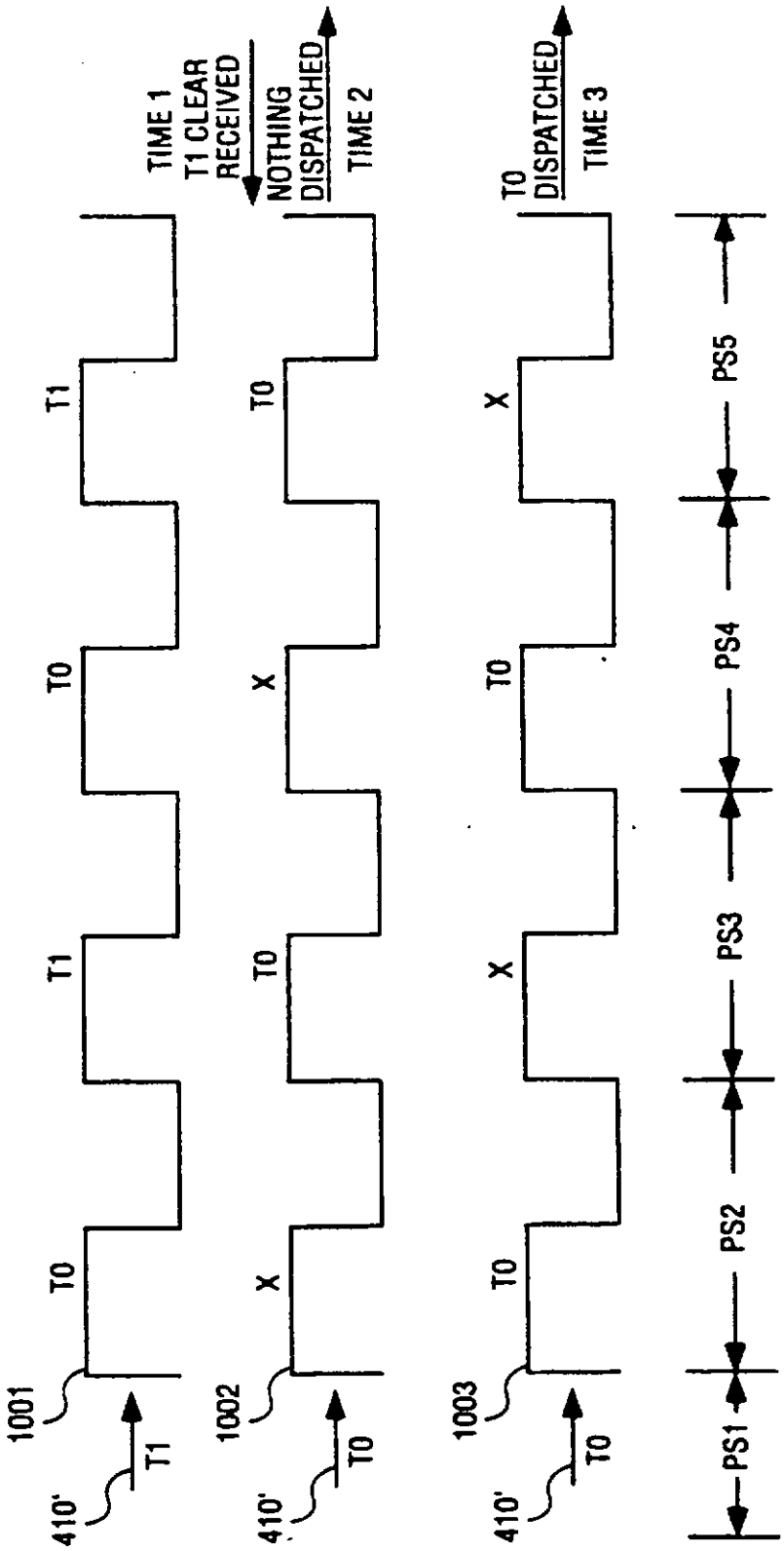

TIME 1
T1 CLEAR RECEIVED
NOTHING DISPATCHED
TIME 2
T0 DISPATCHED
TIME 3
1001
1002
1003
410'
T1
T0
T0
T0
T1
T1
T0
X
T0
X
T0
X
T0
X
PS1
PS2
PS3
PS4
PS5

FIG. 10

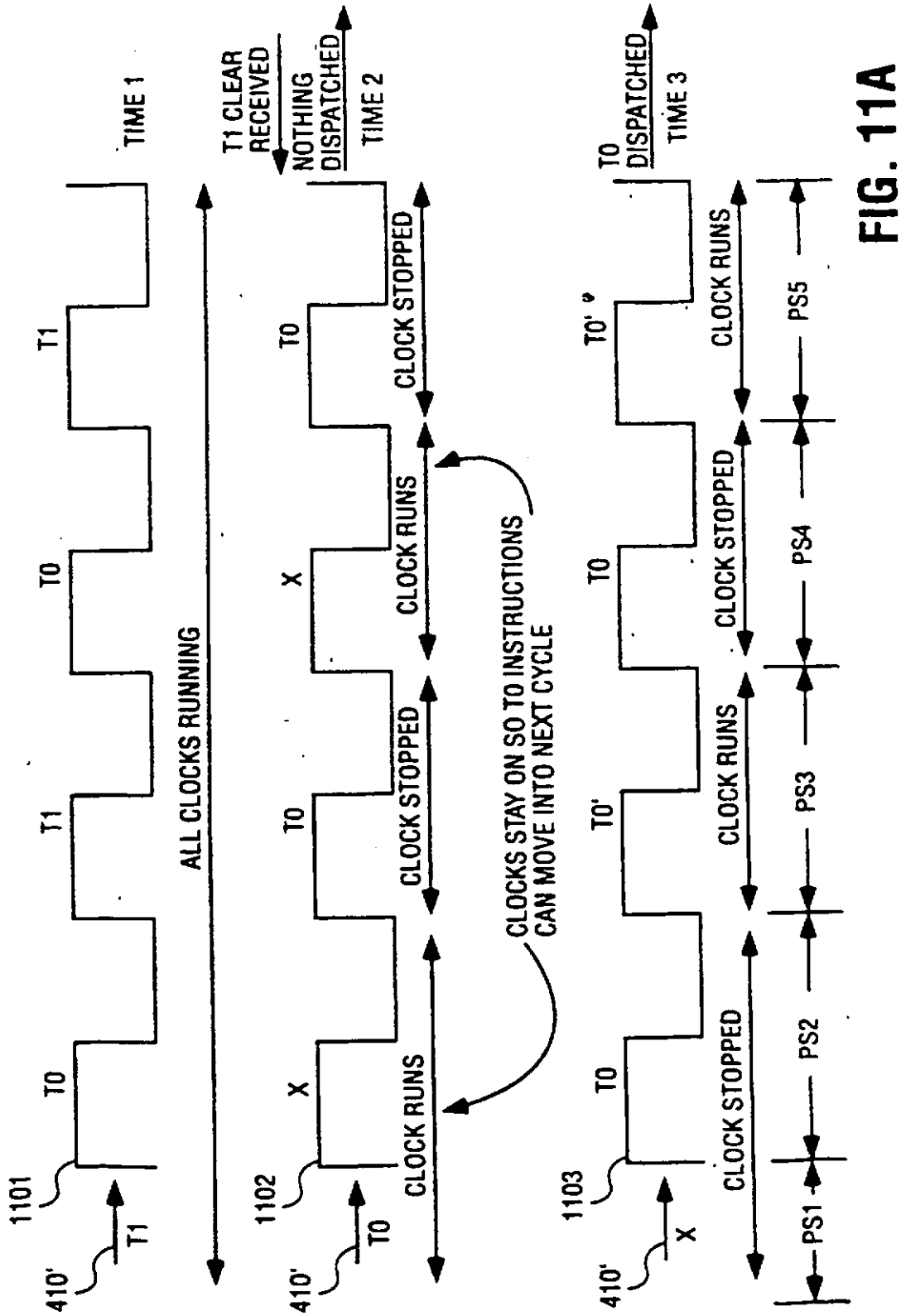

TIME 1
T1 CLEAR RECEIVED
NOTHING DISPATCHED
TIME 2
T0 DISPATCHED
TIME 3
ALL CLOCKS RUNNING
CLOCKS STAY ON SO TO INSTRUCTIONS CAN MOVE INTO NEXT CYCLE
CLOCK RUNS
CLOCK STOPPED
1101
1102
1103
410'
T1
T0
T0'
T0''
X
PS1
PS2
PS3
PS4
PS5

FIG. 11A

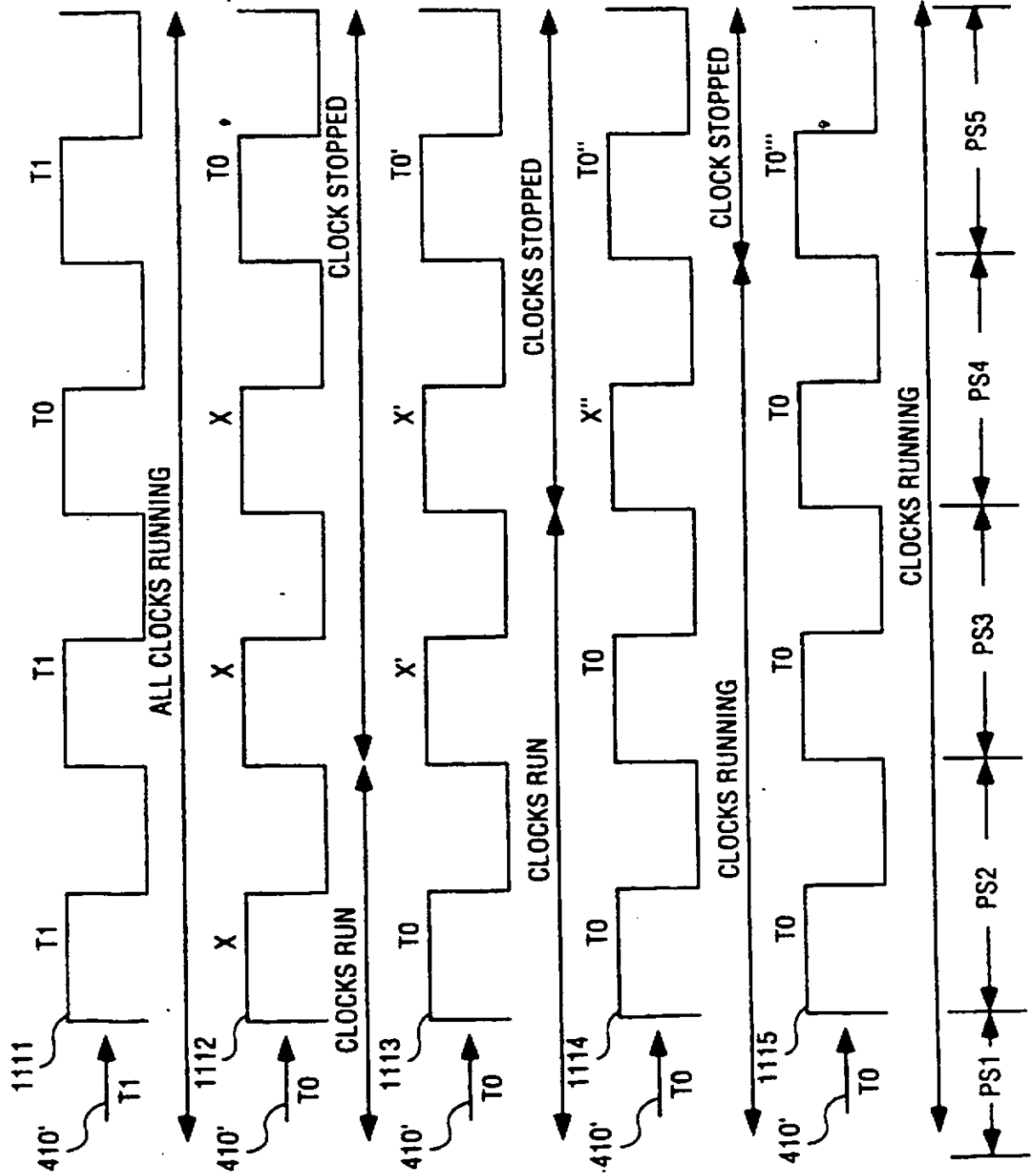

TIME 1
T1 CLEAR RECEIVED
NOTHING DISPATCHED
TIME 2
T0 DISPATCHED
TIME 3
NOTHING DISPATCHED
TIME 4
NOTHING DISPATCHED
TIME 5
ALL CLOCKS RUNNING
CLOCK STOPPED
CLOCKS RUN
CLOCKS STOPPED
CLOCKS RUN
CLOCK STOPPED
CLOCKS RUNNING
CLOCKS RUNNING
T1
T0
X
X'
X''
T0'
T0''
T0'''
1111
1112
1113
1114
1115
410'
PS1
PS2
PS3
PS4
PS5

FIG. 11B