

Abstract

FULLY SILICIDE CASCADED LINKED ELECTROSTATIC DISCHARGE PROTECTION

A method and a structure of for an Electro Static Discharge (ESD) device that is silicided. There are three preferred embodiments of the invention. The first embodiment has a N/P/N structure. The emitter, the collector and the substrate form a parasitic transistor and the substrate is connected to the p+ diffusion region. The emitter and the substrate act as a first diode D1 and the collector and the substrate act as a second diode D2. The second embodiment has a first N+ well between a second n+ (collector) region and a P+ base region. The V_{t1} is controlled by the dopant profiles of the P+ base and the n- first well where they intersect. The third embodiment is similar to the second embodiment, but the n-well covers all of drain. A parasitic NPN bipolar transistor comprises: an emitter, a parasitic base and a drain. The emitter is formed by the first n+ region. The parasitic base is formed by the p-substrate. The collector is formed by the second n+ region and the first n- well. The V_{t1} is controlled by the dopant profiles of the P+ base and the n- first well where they intersect.

(FIGURE 1A IS SUGGESTED FOR PUBLICATION)