

## ATM CELL EXCHANGE

### BACKGROUND OF THE INVENTION

#### Filed of the Invention

5           The present invention relates to an ATM (Asynchronous Transfer Mode) exchange which is provided with a function of exchanging ATM cells.

#### Description of the Prior Art

          There has been widely used an ATM exchange that exchanges  
10   cells which are fixed-length packets. To exchange the cells, the ATM exchange requires a buffer memory for temporally storing them. Concerning arrangement and number of the buffer memory, there have been proposed a variety of exchanging methods. Several exchanging methods have been discussed in the following references: (1)  
15   "Development of a high-speed ATM exchange system", NTT R&D Vol. 95 No. 10 p. 839 - 846; and (2) "Method of configuring 160 Gigabit/s ATM exchange with a switch changing a link-speed" SSE 93-69, IN 93-76, CS 93-92 (1993-10).

          More definitely, this invention relates to an output buffer type  
20   ATM exchange. Hereinafter, the output buffer type ATM exchange will be discussed first. An explanation of an ATM exchange with multiple steps (e.g., an ATM exchange with three steps shown in Fig. 12), which has some drawbacks in contrast with the output buffer type ATM exchange, will follow in order to clarify advantages of the output buffer  
25   type ATM exchange, which will proceed focusing on the disadvantages of the ATM exchange with multiple steps.

          To summarize the following discussion, the conventional output



buffer type ATM exchange shown in Fig. 11 (a) has solved the disadvantages of the ATM exchange with multiple steps shown in Fig. 12, that is to say, cell collisions. In the conventional output buffer type ATM exchange in Fig. 11(a), the cells on the common bus 1205 are required to  
5 run at extremely high speed, which gives some difficulties, such as limitation on selecting devices, in designing the output buffer type ATM exchange. Therefore, the output buffer type ATM exchange according to this invention removes such difficulties. To attain the object, the principal architecture of the output buffer type ATM exchange in  
10 accordance with this invention is as following: as shown in Fig. 1, the cells output from "one" input unit are distributed or divided into "a plurality of" output units. Furthermore, the present invention employs the parallel expansion, which increases the number of the lines on which the cells runs. The parallel expansion allows the cells to run at low  
15 speed.

Hereinbelow, a conventional output buffer type ATM exchange will be explained, as an example of exchanging methods with reference to Fig. 11, which shows  $n$  by  $n$  output buffer type ATM exchange ( $n$  denotes the number of input lines and output lines). As shown in Fig. 11 (a), each of  
20 the input cells 1200-1 to 1200- $n$  are fed into the respective input cell processors 1200-1 to 1200- $n$  via the input line 1201-1 to 1201- $n$ . The input cell processors 1202-1 to 1202- $n$  each make the input cells 1200-1 to 1200- $n$  be in phase, and implement bit expansion thereon, thus outputting the cells which have experienced the bit expansion, to the cell  
25 multiplexer 1204 via the lines 1203-1 to 1203- $n$ . The cell multiplexer 1204 performs time division multiplex on the cells, thereby delivering the cells which have undergone the time division multiplex, to the output



buffers 1206-1 to 1206-n via the common bus 1205.

In Fig. 11 (b), each of the output buffers 1206-1 to 1206-n incorporates the destination reference unit 1209 and the buffer memory 1210. The destination reference unit 1209 identifies the cells on the common bus 1205, to write only the cells directed to the respective buffer memory 1210 therein, whereby each buffer memory 1210 stores the cells directed thereto with the other cells not stored therein.

With respect to the length of the cells, the ITU-T recommendation and the ATM forum defines 53 byte. In most ATM exchanges, at the head of the 53 byte cell is added one byte, which is destination information designating the destination of the output buffer, whereby the 54 byte cell is exchanged. In Fig. 11 (a), the length of the cells 1200-1 to 1200-n is 54 byte.

Fig. 11 (c) shows the format of the 53 byte cell 1300, which is defined in the ITU-T recommendation and the ATM forum, while showing the format of the 54 byte cell 1301, which is added one byte 1302. In case of the 54 byte cell, the output buffers 1206-1 to 1206-n are necessitated to be larger, as compared with those of the 53 byte cell 1300. In addition, since the throughput a cell unit is larger, memories for speed control of the cells are necessary.

Incidentally, spreading of multimedia communication requires a high speed and large scale ATM exchange. The capacity of current ATM exchanges ranges from 10 Gbps to 20 Gbps, whereas the necessary capacity of the future ATM exchanges is approximately 100 Gbps.

As one of the schemes of developing the large scale and high speed ATM exchange, there has been known a method of connecting a plurality of switches of 10 - 20 Gbps exchange capacity, as disclosed in the



references (1) and (2). An ATM exchange with three steps is illustrated in Fig. 12. This ATM switch comprises the unit switches 1420 to 1450 at the first step, the unit switches 1421 to 1451 at the second step, and the unit switches 1422 to 1452 at the third step. Here, the unit switch 1420, for example, accommodates input lines 1400-1 to 1400-m. Similarly, the other unit switches 1430, 1440, and 1450 accommodate the input lines 1401-1 to 1401-m, 1402-1 to 1402-m, and 1403-1 to 1403-m, respectively. On the contrary, at the third step, for example, the unit switch 1422 accommodates the output lines 1404-1 to 1404-m. Similarly, the other unit switches 1432, 1442, and 1452 accommodate the output lines 1405-1 to 1405-m, 1406-1 to 1406-m, and 1407-1 to 1407-m, respectively. At the second step, the unit switch 1421 is connected to the unit switches 1420 and 1430 via the respective lines 1411 and 1412, while being connected to the unit switches 1422 and 1432 via the respective lines 1413 and 1414. The other unit switches 1431, 1441, and 1451 are connected likewise. The ATM exchange has some problems as follows.

(1) The throughput in a link, or between a unit switch and the following unit switch must be fast. For example, assuming that the throughput of each input line is  $V$ , the throughput of each link is  $m \times V$ . More specifically, provided that the throughput of each of the input lines is 155.52 Mbps, and the number thereof is eight, the throughput of the link is approximately 1.2 Gbps. This represents that the unit switch increases in the throughput, or the operating frequency, with further increasing of the number of the input lines and throughput thereof. Accordingly, the unit switch must write such fast cells therein.

With respect to devices, in comparison with the ECL (Emitter



Coupled Logic) and TTL (Transistor transistor Logic), the CMOS (Complementary Metal-Oxide-Semiconductor) generally favors large scale integration of the ATM switch in manufacturing and cost. However, the CMOS does not enable the integrated ATM switch to operate beyond 150  
5 MHz, and also gives several restrictions on circuit designing relevant to delay and layout.

Furthermore, concerning the memory, it is difficult to store large amount of cells therein at extremely high speed, for example, 150 MHz. Also, the power consumption of the memory increases with further  
10 increase of the operating frequency thereof. Hence, it is difficult to employ the ECL and the TTL in large scale integration of the memory in lieu of the CMOS in terms of operating speed and power consumption.

(2) In order to reduce the throughput of the links, there have been proposed a method of making each link in parallel and another method of  
15 increasing the number of the links between the unit switches. These methods, however, may gain the number of wiring among the unit switches. For example, providing that each unit switch integrated in a LSI and LSIs are mounted on a printed wiring board, many wirings among the LSIs may be troublesome. In addition, crosstalk among the  
20 wirings and delay of the cells deteriorate with further high operation speed of the links.

Increasing the number of the links allows the unit switches to select the links more freely, which appears to avoid the above collisions. This increases the number of the paths including a plurality of links (e.g.,  
25 the paths 1408, 1409 and 1410) through which each cell can pass. However, the increase of the paths makes it difficult for each unit switch to judge which of the paths is selected. Furthermore, it is difficult to



configure algorithm for selecting an appropriate path with no cell collision, and if possible, this leads to increasing of the hardware.

(3) There may occur collisions of the cells at the output points of the unit switches of the second step and other following switches. More  
5 definitely, assuming that the cells through the input line 1400-1 arrive at the output line 1406-1 while the cells through the input line 1402-1 arrive at the output line 1406-1, the former cells advances along the path 1408 and the latter cells advances along the path 1409. If both cells are fed in the unit switches 1420 and 1440, those cells collide with each  
10 other at the output point 1415 of the unit switch 1431 or at the buffer memory therein. Similarly, the cells through the input line 1403-m advances along the path 1410, whereby another collision may arise at the output point 1416 of the unit switch 1442 or the buffer memory thereof. Therefore, cascading a plurality of unit switches requires avoiding such  
15 collisions of the cells, which burdens the hardware of the unit switches with a large quantity of algorithm for avoidance.

(4) In case of cascading of a plurality of unit switches, there is required a trigger signal from a following unit switch to a preceding unit switch, wherein the control signal instructs the preceding unit switch to  
20 output the cells therefrom. Consequently, this further increases the number of wirings between neighboring unit switches. For example, in case of transferring the cells between the unit switch 1420 and the unit switch 1421 via the link 1411, the control signal 1417 originated by the unit switch 1421 serves to request the unit switch 1420 to output the  
25 cells to the unit switch 1421.

On the contrary to cascading a plurality of unit switches, the single switch, such as the output buffer type switch and the common



buffer type switch, appear to be preferable. However, these single switches requires multiplexing the input cells. Accordingly, this necessitates high speed operation in transferring and writing.

## 5 SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide an ATM cell exchange capable of exchanging cells at high transmission rate and with few cells discarded.

According to one aspect of the present invention, there is provided  
10 an output buffer type ATM cell exchange comprising: an input unit distributing a plurality of incoming cells having destination information which denotes a destination for each cell; a buffer unit buffering the distributed cells; and a plurality of output units performing parallel reduction on the distributed cells.

15 According to another aspect of the present invention, there is provided a sub-buffer unit in a buffer unit of an output buffer type ATM exchange which buffers incoming cells having destination information for each cell, the sub-buffer unit comprising: a buffer memory temporarily storing the incoming cells; an address filter unit assigned a given  
20 destination information, including a plurality of parallel expansion circuits implementing an parallel expansion on the incoming cells, a cell multiplexer implementing a multiplex on the parallel-expanded cells, and a write controller allowing a cell of the parallel-expanded cells to be written into the buffer memory upon judging that the destination  
25 information of the cell is coincident with the given destination information; and a reduction circuit implementing a parallel reduction on a cell output from the buffer memory.



According to further another aspect of the present invention, there is provided a method of exchanging a plurality of cells which have destination information and pass one of a plurality of buffer memories having given destination information in an output buffer type ATM  
5 exchange, the method comprising the steps of: comparing the destination information contained in a cell with the given destination information; and allowing the cell having the same destination information as the given destination of a buffer memory to be stored into the buffer memory.

## 10 BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be understood more fully from the detailed description given hereinbelow and from the accompanying drawings of the preferred embodiment of the invention, which, however, should not be taken to limit the invention to the specific embodiment but  
15 are for explanation and understanding only.

In the drawings:

Fig. 1 is a schematic diagram showing the configuration of the first embodiment of the ATM cell switch according to the present invention;

20 Fig. 2 is a schematic diagram showing the configuration of the input unit;

Fig. 3 is an explanatory diagram showing the operation of the input unit;

Fig. 4 is a diagram showing the operation of the phase adjusting  
25 unit in the input unit;

Fig. 5 is a diagram showing detailed configuration of the sub-buffer unit in the buffer unit;

Fig. 6 is an explanatory diagram showing the operation of the sub-buffer unit;

Fig. 7 is an explanatory diagram showing the operation of the FIFO in the buffer memory and the operation of the parallel expansion  
5 circuit;

Fig. 8 is a schematic diagram showing the configuration of the output unit;

Fig. 9 is an explanatory diagram showing the operation of the output unit;

10 Fig. 10 is a schematic diagram showing the configuration of the sub-buffer unit in the second embodiment of the ATM switch;

Figs. 11 (a) to (c) are diagram showing a conventional ATM switch; and

Fig. 12 is an explanatory diagram showing the operation of the  
15 conventional ATM switch.

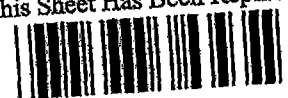
## DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, the preferred embodiments of the ATM switch according to the present invention will be now described with reference to  
20 the accompanying drawings.

<First Embodiment>

<configuration>

Fig. 1 is a diagram showing the configuration of the first embodiment of the ATM switch, which is an output buffer type of  $n$  input  
25 lines by  $n$  output lines. As shown in Fig. 1, the ATM switch incorporates a plurality of input units 1-1 to 1-( $n/m$ ), a plurality of buffer units 2-A to 2-D, and a plurality of output units 3-1 to 3- $n$ , where  $m$  denotes the



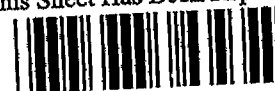
number of lines of input cell fed into each of the input units 1-1 to 1-(n/m). Assuming  $m = 16$  and  $n = 128$ , the ATM switch requires 8 (=  $128/16$ ) input units. Herein, all of the input units 1-1 to 1-(n/m) work similarly to each other, and all of the buffer units 2-A to 2-D work  
5 similarly to each other, and all of the output units 3-1 to 3-n work similarly to each other. The explanation will advance in order of the input units 1-1 to 1-(n/m), the buffer units 2-A to 2-D, and the output units 3-1 to 3-n.

<input unit>

10 First, the input cells 4-1(1) to 4-1(m) are fed to the input unit 1-1, and the other input cells are similarly fed to the other input units. Herein, for example, the input unit 1-1 executes the parallel expansion, which is a function of dividing serial input cells into a plurality of cells using a plurality of parallel signal lines, on the input cells 4-1(1), thus  
15 outputting them through the line 5-1(1) including four lines 5-1(1)(A) to 5-1(1)(D). Similarly, the other input units executes the parallel expansion on the respective input cells. Furthermore, the input unit 1-1 multiplexes each first octet in each input cells 4-1(1) to 4-1(m) to output the multiplexed cells via the line 6-1.

20 <buffer unit>

Next, The main function of each of the four buffer units 2-A to 2-D is to buffer the cells which have undergone the parallel expansion in the input units 1-1 to 1-(n/m). For example, the buffer unit 2-A includes  $n$  sub-buffer units 2-A(1) to 2-A( $n$ ), wherein these  $n$  sub-buffer  
25 units 2-A(1) to 2-A( $n$ ) are used to divide the input cells into  $n$  cells. For example, the parallel-expanded cells via the line 5-1(A) are divided into the  $n$  sub-buffer units 2-A(1) to 2-A( $n$ ). Similarly, in the buffer unit 2-A,



each of the cells input from the input units 1-1 to 1-(n/m), experiences n-branching to be divided into the n sub-buffer units 2-A(1) to 2-A(n).

As stated above, the cells output from the input unit 1-1 to the buffer unit 2-A via the line 5-1(1)(A), are commonly distributed to the sub-buffer units 2-A(1) to 2-A(n). Similarly, the cells via the line 5-1(1)(B), the cells via the line 5-1(1)(C), and the cells via the line 5-1(1)(D) are commonly distributed to the sub-buffer units (not shown) in the respective buffer units 2-B, 2-C, and 2-D. The cells output from the other input units are distributed similarly to the cells output from the input unit 1-1.

The first octet output on the line 6-1 which has been m multiplexed in each of the input unit 1-1, is input, for example, into each of the n sub-buffer units 2-A(1) to 2-A(n) in the buffer unit 2-A, and similarly is input in each of the sub-buffer units in the other buffer units 2-B to 2-D. Similarly, the first octet outputs on the lines other than the line 6-1, which each have experienced m multiplex in the respective input units, are input in each of the n sub-buffer units in the buffer units 2-A to 2-D.

Incidentally, for example in the buffer unit 2-A, the sub-buffer units 2-A(1) serves to exchange the cells input through the m lines 5-1(1)(A) to 5-1(m)(A) based on the first octets input via the lines 6-1, wherein the exchanged cells are output to the output unit 3-1 via the line 7-1(A). The other sub-buffer units in the buffer unit 2-A work similarly, and further the sub-buffer units in the other buffer units 2-B to 2-D works similarly.

<output unit>

For example, the output unit 3-1 is fed with the exchanged cells

from the buffer unit 2-A via the line 7-1(A), and is similarly fed with the other exchanged cells from the buffer units 2-B to 2-D via the lines 7-1(B) to 7-1(D), respectively, wherein the output unit 3-1 gathers those cells to output them via the line 8-1. More specifically, the output unit 3-1  
5 generates new cells using the input cells to provide the new cells via the line 8-1. The other output units operate similarly.

<operation>

Hereinbelow, the switching operation of the first embodiment of the ATM switch will be described in order of the input unit, the buffer unit,  
10 and the output unit. For easy understanding, in the following explanation, it is assumed  $m=8$  and  $n=64$ . More definitely, the ATM switch is an output buffer type switch accommodating 64 input lines and 64 output lines, and having 2.5 Gbps transmission rate. Each input unit accommodates eight lines, which denotes the number of the input  
15 units is also eight ( $=64/8$ ). The number of the buffer units is four, wherein each buffer unit incorporates 64 sub-buffers, which denotes there are totally 256 ( $=64*4$ ) sub-buffers in the system. The number of the output units is 64 similarly to the number of the output lines. Finally, the format of the input cells and the output cells is identical with  
20 that of the cells 1301 in Fig. 11 (c), which is added the destination information 1302 to the cells 1300 regulated in the ITU-T and the ATM forum.

<input unit>

Hereinafter, the operation of the input unit will be described  
25 referring Figs. 2 and 3 each illustrating the detailed configurations thereof. First, the input cells 4-1(1) to 4-1(8) and the frame signals 9-1(1) to 9-1(8) are input to the phase adjusting unit 11. Here, the frame



signal 9-1 is defined as the reference signal having the fixed-length data for identifying the header of each cell. Each pair of an input cell and a frame signal is synchronizing, and more definitely, the input cell 4-1(1), the frame signal 9-1(1), and the clock used therefor are in phase shown in  
5 Fig. 3. In addition, the input cells are fed in eight parallel; therefore, the operation frequency of the clock is approximately 310 MHz (= 2.5 Gbps/8).

Incidentally, all of the input cells do not always synchronize with each other and all of the frame signals do not likewise. For example, the  
10 input cell 4-1(1) and the input cell 4-1(8) are not always in phase, and the frame signal 9-1(1) and the frame signal 9-1(8) are not always in phase. The reason is as following: though those cells flow pursuant to the same clock, there arise some phase errors of the clock among the cells. Accordingly, the ATM switch need to make all of the input cells be in  
15 synchronization with each other, using the built-in common clock. The phase adjusting unit 11 makes the input cells be in phase as shown in Fig. 4. Among the methods of adjusting the phases of the input cells, there are some methods of (1) adjusting based upon a given line (e.g., the smallest line number), (2) adjusting based upon the input line containing  
20 the earliest cell, and (3) adjusting based upon an independent clock prepared in the phase adjusting unit 11. Consequently, the synchronized input cells 4-1(1) to 4-1(4) and frame signals 9-1(1) to 9-1(4) are output to the destination extracting units 13-1(1) to 13-1(8), and the signal relevant to the phase adjustment is output the timing/frame  
25 generating unit 12.

Responding to this signal, the timing/frame generating unit 12 generates the control signal for use in internal circuits of the input unit



1-1 and the frame signal 16-1 used for identifying header of the cells output from the input unit 1-1 at the clock frequency 155 MHz.

The synchronized cells are also input to the parallel expansion units 14-1(1) to 14-1(8), wherein the parallel expansion circuits 14-1(1) to 14-1(8) execute parallel expansion on the input cells, thus allowing the input cells to convert from 8 parallel to 16 parallel, which indicates that the frequency of clock frequency halves from 310 MHz to 155 MHz. For example, in the parallel expansion circuit 14-1(1), the cells expanded in 16 parallel are distributed to the buffer units 2-A to 2-D as the output cells 10-1(1)(A) to 10-1(1)(D) via the lines 5-1(1)(A) to 5-1(1)(D) in units of 4 parallel, respectively. Here, the parallel expansion is implemented as shown in Fig. 3. More specifically, at the first octets 1 to 54 in the input cell each are divided into the upper bits and the lower bits, wherein for example, the output cell 10-1(1)(A) involving the lower bits of the even number, is generated. Thereafter, each of the output cells 10-1(1)(A) to 10-1(1)(D) shown in Fig. 3 are respectively output to the buffer units 2-A to 2-D.

The destination extracting unit 13-1(1), for example, extracts the first octet of each input cell to output it to the destination multiplexing unit 17, wherein the destination multiplexing unit 17 multiplexes the first octets, thereby outputting it to the buffer unit 2-A as the destination information 18-1 with respect to the input unit 1-1, at the same clock frequency 155 MHz as that of the output cells 10-1(1)(A) to 10-1(1)(D). Besides, the destination information 18-1 is commonly output to the buffer units 2-B to 2-D. The first octets of input cells 4-1(1) to 4-1(8) are multiplexed in ascending order of line numbers to be the destination information 18-1 as shown in Fig. 3. Here, the system involving 8 lines



requires 8 bytes in order to designate 8 addresses thereof while the reserved bytes (RES) will be additionally available for the system involving 16 lines. In addition, as shown in Fig. 3, the frame signal 16, the output cells 10-1(A) to 10-1(D), and the destination information 18-1  
5 synchronize with each other.

<buffer unit>

Fig. 5 is a block diagram showing the detailed configuration of the sub-buffer unit 2-A(1) in the buffer unit 2-A, and Figs. 6 and 7 are explanatory diagrams showing the operation of the sub-buffer unit 2-A(1).  
10 In Fig. 5, the input cells 10-1(1)(A)~10-1(8)(A) to 10-8(1)(A)~10-8(8)(A), the destination information 18-1 to 18-8, and the input unit frame signal 16-1 to 16-8 are fed to the phase adjusting unit 20, wherein there are laid some phase errors of the clock among those signals. The phase  
15 adjusting unit 20 allows those signals to be in phase with each other, thereby outputting the synchronized cells and frame signals to the address filter units 22-1 to 22-8. Based upon the information denoting the synchronization of those signals in the phase adjusting unit 20, which is output therefrom, the timing/frame generating unit 21 generates the control signal 23 and the frame signal 24 of the sub-buffer  
20 unit 2-A(1). The frame signal 24 is used for identifying the header of the cells output from the sub-buffer unit 2-A(1).

The address filter units 22-1 to 22-8 are fed with the cells corresponding to the 64 lines and the destination information in synchronization, wherein for example, the address filter unit 22-1 is fed  
25 with the cells corresponding to 8 lines. In the address filter unit 22-1, the cells enter the parallel expansion circuits 25-1(1) to 25-1(8) in 4 parallel in synchronization with the 155 MHz clock frequency, wherein



the cells in 4 parallel undergoes parallel expansion in the parallel expansion circuit 25-1(1), for example, more definitely, the line number of the cells increases from 4 parallel to 108 parallel. On the contrary, the operation frequency of the cells reduces from 155 MHz to 5.76 MHz. The  
5 clock having 5.76 MHz is given by the timing/frame generating unit 21. As shown in Fig. 6, the input cell 10-1(1)(A) in 8 parallel, for example, experiences parallel expansion in synchronization with the 5.76 MHz clock, thereby developing to 108 parallel at 52 MHz.

Subsequently, the cells in 108 parallel are fed into the cell  
10 multiplexer 26-1, wherein the cell multiplexer 26-1 implements 9 multiplex on the cells output from the parallel expansion circuits 25-1(1) to 25-1(8), and also synchronizes them with the 52 MHz clock frequency. This clock is generated by the timing/frame generating unit 21. Here, the reason why the 9 multiplexing is executed is to give a time for reading  
15 cells out of buffer memories, which will be described in detail later.

Hereinafter, the multiplexing in the cell multiplexer 26-1 will be described. In Fig. 6, the internal reference signal serves to identify the smallest line number of cells in the cell multiplexer 26-1, which is generated in the timing/frame generating unit 21. The multiplexed cells  
20 denotes the cells which have undergone parallel expansion in 108 parallel, wherein the cells are multiplexed in ascending order from the smallest number to the largest number. The area READ is an area for reading cells out of the buffer memory 30, wherein the area READ does not involve any cells.

25 Meanwhile, the destination information output from the phase adjusting unit 20, for example, is fed to the destination information processor 27-1 in the address filter unit 22-1. The destination

information processor 27-1 makes the destination information synchronizing with the 155 MHz synchronize with the 52 MHz clock. In short, the destination information output from the destination information processor 27-1 synchronizes with the 52 MHz clock and the position of the header of the destination information agrees with the starting position (SP) of the internal reference signal, which is required in writing cells into buffer memory 30. The write controller 28-1, for example, generates the write enable signal (WES) for memory writing. The write controller 28-1 needs to comprehend which of 64 output lines it should corresponds to. To meet this requirement, to the write controller 28-1 is given the destination set signal 29 denoting which line it correspond to. Furthermore, to all of the write controllers in a sub-buffer unit is given the common set signal. More definitely, the destination set signal 29 is shared by all of the write controllers 28-1 to 28-8 in the sub-buffer unit 2-A(1). In addition, the same destination set signal 29 is fed into the other sub-buffer units 2-B(1) to 2-D(1), wherein the functions of write controllers (not shown) therein are the same as that of the write controller 28-1 in the sub-buffer unit 2-A(1).

Returning to the cell 1301 in Fig. 11 (c), the data "destination" in the destination information byte 1302 denotes the number of output line through which the cell 1301 should pass. The write controller 28-1 compares the destination laid in the cell output from the destination information processor 27-1, with the destination specified by the destination set signal 29. If identical, the write controller 28-1 validates the write enable signal (WES), whereby the cell is permitted to advance to the buffer memory 30. Here, assuming that the destination set signal 29 denotes "1" but the destinations laid in the cells 1301 in Fig. 11 (c) are "1",



"1", "5", "1", "64", "1", "1", and "8", the respective cells are given "OK", "OK", "NG", OK, "NG", "OK", "OK", and "NG" as the write enable signal (WES), whereby the cells given "OK" are permitted to be written in the buffer memory 30 in the sub-buffer unit 2-A(1). More specifically, the 1st cell,  
5 the 2nd cell, the 4th cell, the 6th cell, and the 7th cell are permitted to be written therein.

On the contrary, the cell with the destination number "5" is written into the buffer memory for the 5th line (not shown), the cell with the destination number "64" is written into the buffer memory for the  
10 64th line (not shown), and the cell with the destination number "8" is written into the buffer memory for the 8th line (not shown). Therefore, all of the cells contained in the one cell period, are always written into one of the buffer memories. This indicates that all of the cells for the 64 lines input during the one cell period can be stored.

15 Besides, the external read enable signal (ERES) serves to read out data from the buffer memory. Herein, both of the dual port memory and the single port memory are basically available for the buffer memory, as long as the external read enable signal (ERES) is provided. There is, however, a difference therebetween. Employing the dual memory as the  
20 buffer memory does not require the external read enable signal (ERES) to be laid at a specific time of period, which allows the external read enable signal (ERES) to be positioned anywhere. In contrast to this, employing the single memory as the buffer memory requires the external read enable signal (ERES) to be laid at the specific time of period, more  
25 definitely, at the time of period differing from the time of period to which the write enable signals (WES) are assigned. Therefore, the ninth bit allocated to the time of period following the time of period for the write



enable signals (WES) enables the single port memory to read out the data therefrom as well as the dual port memory.

The buffer memory 30 incorporates, for example, eight FIFOs 32-1 to 32-8 (First-in First-out) including eight write ports and one read port. The buffer memory 30 is fed with the cells from the cell multiplexer 26-1. Also, the buffer memory 30 is fed with the write enable signal (WES) from the write controller 28-1, wherein the write controller 28-1 is provided with the buffer full notification signal (BFN) 31-1 notifying the address filter unit 22 that the buffer memory is full with cells. The buffer full notification signal (BFN) is output from the buffer memory 30. The buffer full notification signal (BFN) serves to inhibit the address filter unit 22-1 to 22-8 from writing cells beyond the storage capacity of the buffer memory 30. Therefore, for example, the write controller 28-1 does not allow the cells to be written in the buffer memory 30 upon receipt of a "NG" buffer full notification signal (BFN) 31-1, that is, invalidates the write enable signal (WES1) 101-1. That indicates that overwriting the cells into the buffer memory 30 is inhibited while the cells are discarded upon inhibition of writing the cells.

Incidentally, as shown in Fig. 7, the accumulated cell 33 during one cell period is laid in the FIFO 32-1. In this case, the cell non-accumulation signal (CNA) 34-1, for example, denotes whether or not the cells are accumulated in the FIFO 32-1. The selector 35 serves for selection of the multiplexed cells output from the FIFOs 32-1 to 32-8, thus outputting the selected cells (SC). The external read enable signal (ERES) 36 is given by the read controller 37.

In the memory buffer 30 configured as described above, the multiplexed cells (MC) 100-1 to 100-8 are written according to the write

enable signals (WES) 101-1 to 101-8. As stated hereinbefore, the 1st, 2nd, 4th, 6th, and 7th cells are permitted to be written into the buffer memory 30, namely, into the FIFO 32-1. The cells are written during one cell period.

5           In case of reading the cells, at first the selector 35 selects one among the multiplexed cells 102-1 to 102-8 output from the FIFO 32-1 to 32-8. Next, the selector 35 outputs the selected cells at the time that the external read enable signal (ERES) is "OK" as shown in Fig. 6. In order to permit the FIFO 32-1 corresponding to the 1st cell 33-1 of the selected  
10 cells 33 to output the cell 33-1, the selector 35 gives the FIFO 32-1 a "valid" read enable signal (RES1), wherein the 1st cell 33-1 is output in synchronization with the 5.76 MHz clock frequency. Assuming that the FIFO 32-2 (not shown) outputs the 1st cell 38-1 laid at the top of the accumulated cells stored therein similarly to the 1st cell 33-1, the 1st cell  
15 38-1 is output in synchronization with the 5.76 MHz clock frequency and further the time of period between the cell 33-1 and the cell 38-1 is the one cell period. In this way, all of the cells stored in the FIFOs 32-1 to 32-8 are in turn output at interval of one cell period. In this procedure, if storing no cell to be output, the FIFO is skipped. Whether or not the  
20 FIFOs 32-1 to 32-8 each store any cell to be output, is notified to selector 35 using the cell non-accumulation signal 34-1 to 34-8.

          In Fig. 5, the selected cell (SC) output from the buffer memory 30 is fed to the parallel reduction circuit 40. The parallel reduction circuit 40 executes on the input cell (SC) a parallel reduction, which is a function  
25 opposite to the parallel expansion, thus converting it from 108 parallel at 5.76 MHz to 4 parallel at 155 MHz, as shown in Fig. 7. Since the sub-buffer unit 2-A(1) handles processes related to the output line 1, the cells



output from the parallel reduction circuit 40 in the sub-buffer unit 2-A(1) is directed to the output unit 3-1 that operates for the processes related to the output line 1, wherein transmission of the output cells 41 starts at the header of the frame signal (low bit) as shown in Fig. 7.

5 <output unit>

Fig. 8 shows the detailed configuration of the output unit 3-1. The output unit 3-1 comprises the phase adjusting unit 50, the parallel expansion circuit 51, and the frame generating unit 52. The phase adjusting unit 50 is, for example, fed with the input cell 7-1(A), which is  
10 the same as the output cell 41, and the frame signal 42 from the parallel reduction circuit 40 in the sub-buffer unit 2-A(1), while being fed with the other input cells and the corresponding frame signals likewise. Since the phases of the input cells are slightly different from each other, the phase adjusting unit 50 permits the input cells to be in phase.  
15 Thereafter, the input cells are given to the parallel expansion circuit 51 while the notification signal 53 which denotes of the synchronization of the input cells, is given to the frame generating unit 52 from the phase adjusting unit 50. Responding to the notification signal 53, the frame generating unit 52 generates the frame signal 55. As shown in Fig. 9,  
20 the parallel expansion circuit 51 performs parallel reduction on the input cells 7-1(A) to 7-1(D), thus converting the cells from 16 parallel (4 parallel x 4) at 155 MHz to 8 parallel at 310 MHz at the output cell 54. In this way, the input cells 4-1 (1) to 4-1 (m) which has experienced four-division in the input unit 1-1 are regenerated to the complete cells 8-1 in the  
25 output unit 3-1. In addition, the output cells 54 and the frame signal 53 are in phase.

As described above, the first embodiment of the ATM switch

according to the present invention can reduce the speed of cells passing through the sub-buffer unit of the buffer unit by executing parallel expansion on input cells, thereby decreasing discarded cells. Furthermore, in the sub-buffer unit, the buffer memory notifies the  
5 corresponding address filter unit whether the corresponding FIFO is full of cells or not, and the address filter unit controls storing of cells in the FIFO based upon the notification. Accordingly, the ATM switch can more securely reduce the number of discarded cells because of avoiding overwriting cells. Also, the address filter unit checks destination  
10 information contained in cells that intend to pass through the address filter and to be stored in the corresponding FIFO. If the destination of the cell is different from that of the destination of the address filter unit, the address filter unit does not permit the cell to pass therethrough. In other word, the address filter unit allows only the cell having the same  
15 destination as that thereof; the FIFO can avoid being filled with cells having the other destinations. This leads to reduction of discarded cells.

<Second embodiment>

Hereinafter, the second embodiment of the ATM switch according to the present invention will be described with reference to Fig. 10. In  
20 Fig. 5, assuming that a set is constituted of eight address filter units 22-1 to 22-8 and one buffer memory 30, the sub-buffer unit 2-A(1) in Fig. 10 includes two sets: one set is used for the first line, and the other set is used for the second line. This is the feature of the second embodiment in comparison with the first embodiment. The cells for the first line are  
25 fed into the address filter units of the former set, while the cells for the second line are fed into the address filter units of the latter set. The frame signal is shared by both of the cells. The other components and

the input cells are identical with those of the first embodiment.

Hereinbelow, the operation of the ATM switch of the second embodiment will be described. Since the address filter units 22-1 to 22-8 work for the first line and the address filter units 22-9 to 22-16 work  
5 for the second line, the former address filter units 22-1 to 22-8 are given the number "1" denoting the first line through the destination set signal 29-1, whereas the latter address filter units 22-9 to 22-16 are given the number "2" denoting the second line through the destination set signal 29-2. Consequently, as compared with the first embodiment that  
10 exchanging one line requires four sub-buffer units, the second embodiment realizes exchanging two lines using four sub-buffer units. Therefore, in case of 64 lines, the first embodiment requires 256 (64 x 4) sub-buffer units while the second embodiment requires the half, 128 sub-buffer units. Accordingly, provided that the whole architecture of  
15 one sub-buffer unit is packaged in one LSI, the second embodiment can reduce the number of LSIs (sub-buffer units), thus decreasing the amount of hardware and wiring therebetween and simplifying the configuration of the switch.

---

This Sheet Has Been Replaced





WHAT IS CLAIMED IS:

1. An output buffer type ATM cell exchange comprising:  
an input unit distributing a plurality of incoming cells having  
destination information which denotes a destination for each cell;  
5 a buffer unit buffering the distributed cells; and  
a plurality of output units performing parallel reduction on the  
distributed cells.

2. An output buffer type ATM cell exchange as set forth in claim 1,  
10 wherein the buffer unit includes

comparing means for comparing the destination information for  
each cell with given destination information assigned to the comparison  
means;  
a buffer memory temporarily storing the distributed cells; and  
15 controlling means for allowing a cell to be stored into the buffer  
memory upon judging that the destination information of the cell is  
coincident with the given destination information.

3. An output buffer type ATM exchange as set forth in claim 2, wherein  
20 the buffer memory notifies the controlling means of a signal denoting  
whether or not the buffer memory can store any more cells, and the  
controlling means allows the cell to be stored into the buffer memory  
upon receipt of the signal denoting that the buffer memory can store any  
more cells.

25

4. An output buffer type ATM exchange as set forth in claim 2, wherein  
the controlling means outputs a signal which allows the buffer memory to



store a cell upon judging that the destination information of the cell is coincident with the given destination information.

5. A sub-buffer unit in a buffer unit of an output buffer type ATM  
5 exchange which buffers incoming cells having destination information for each cell, the sub-buffer unit comprising:

a buffer memory temporarily storing the incoming cells;

an address filter unit assigned a given destination information,  
including a plurality of parallel expansion circuits implementing an  
10 parallel expansion on the incoming cells, a cell multiplexer implementing a multiplex on the parallel-expanded cells, and a write controller allowing a cell of the parallel-expanded cells to be written into the buffer memory upon judging that the destination information of the cell is coincident with the given destination information; and

15 a reduction circuit implementing a parallel reduction on a cell output from the buffer memory.

6. A sub-buffer unit in a buffer unit of an output buffer type ATM  
20 exchange as set forth in claim 5, wherein the buffer memory notifies the address filter unit of a signal denoting whether or not the buffer memory can store any more cells, and the write controller allows the cell to be written into the buffer memory upon receipt of the signal denoting that the buffer memory can store any more cells.

25 7. A sub-buffer unit in a buffer unit of an output buffer type ATM exchange as set forth in claim 5, wherein the write controller outputs a signal which allows the buffer memory to store a cell upon judging that





the destination information of the cell is coincident with the given destination information.

8. A method of exchanging a plurality of cells which have destination  
5 information and pass one of a plurality of buffer memories having given destination information in an output buffer type ATM exchange, the method comprising the steps of:

comparing the destination information contained in a cell with the given destination information; and

10 allowing the cell having the same destination information as the given destination of a buffer memory to be stored into the buffer memory.

9. A method of exchanging a plurality of cells as set forth in claim 8,  
wherein the step of allowing includes the step of judging whether or not  
15 the buffer memory can store any more cells.

10. A method of exchanging a plurality of cells as set forth in claim 8,  
wherein the step of allowing includes the step of outputting a write enable  
signal which allows the buffer memory to write the cell therein.

20 11. A method of exchanging a plurality of cells as set forth in claim 10,  
wherein the step of allowing further includes the step of raising a read enable signal among write enable signals which allows the cell stored in the buffer memory to be read out therefrom.

25 12. A method of exchanging a plurality of cells as set forth in claim 11,  
wherein the read enable signal is laid after the plurality of write enable





signals.

This Sheet Has Been Replaced

