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PATENT SPECIFICATION (11) 1 579 419

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(21) Application No. 23717/78 (22) Filed 30 May 1978
(31) Convention Application Nos.
52/070872 (32) Filed 15 June 1977
52/070873
(33) Japan (JP)
(44) Complete Specification published 19 Nov. 1980
(51) INT. CL.³ H01L 27/04
(52) Index at acceptance
H1K 11A3 11A3A 11D1 11D3 11D 1AA1 1AA9 1BC 1CB 1FJ 9R2 GF



(54) IMPROVEMENTS IN OR RELATING TO STATIC INDUCTION TRANSISTOR LOGIC SEMI-CONDUCTOR DEVICES AND INTEGRATED INJECTION LOGIC SEMI-CONDUCTOR DEVICES

(71) We, KABUSHIKI KAISHA DAINI SEIKOSHA, a Japanese body corporate, of 31-1, 6-chome, Kameido, Koto-ku, Tokyo, Japan, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed to be particularly described in and by the following statement: —

This invention relates to Static Induction Transistor Logic semi-conductor devices (hereinafter referred to by the initials SITL) and to Integrated Injection Logic semiconductor devices (hereinafter referred to by the initials IIL) and more specifically to such devices, of integrated laminated circuit construction wherein a level converting transistor is employed in a signal-level converting circuit to convert a level from one part of the circuit to a different level in another part of the circuit.

Integrated structure SITL semi-conductor devices and IIL semi-conductor devices have the advantages that they can be operated at high frequency and with low power consumption and can be made very small and compact. This makes them very attractive for use in cases in which operation over long periods of time by batteries of small capacity are required, notably in battery-driven, small, electronic timepieces such as wrist watches.

An SITL semi-conductor device consists of a lateral PNP transistor which acts as an injector and a longitudinal field effect transistor which acts as a driving transistor. An IIL semi-conductor device consists of a lateral PNP transistor which acts as an injector and a vertical NPN transistor which acts as a driving transistor. In SITL semi-conductor devices and IIL semi-conductor devices, a laminated integrated circuit construction is often used in order to secure operation with small logic-amplitude-levels (such as 0.7V) and to secure effective use of the injection current. It is often required, when a two-part circuit construction is used, to change the signal level in one part of the circuit construction to another level in the other part of the circuit construction by using a transistor to convert the level. SITL and IIL semi-conductor arrangements for achieving this result are known. In such known arrangements the collector of the transistor for converting the level is directly connected to the gate of a longitudinal field effect driving transistor (in the SITL case) or to the base of a vertical NPN driving transistor (in the IIL case) but, in such known arrangements, undesirably large injection currents flow. This is a disadvantage which it is the main object of the present invention to reduce or eliminate and thus obtain an even lower consumption of current.

According to one aspect of the invention there is provided a Static Induction Tarnsistor Logic semi-conductor device having a lateral PNP transistor used as an injector and a vertical field effect transistor used as a driving transistor and constituting a signal level converting circuit of integrated laminated circuit construction on a chip and making use of injection current in said circuit, said circuit including a level converting transistor which converts a signal level from one part of the circuit to a different level in another part of the circuit, wherein a current limiting element is inserted in a connection between the collector of said level converting transistor and the gate of the driving transistor.

According to another aspect of the invention there is provided an Integrated Injection Logic semi-conductor device having a lateral PNP transistor used as an injector and a vertical NPN transistor used as a driving transistor and constituting a signal level converting circuit of integrated laminated circuit construction on a chip

and making use of injection current in said circuit, said circuit including a level converting transistor which converts a signal level from one part of the circuit to a different level in another part of the circuit, wherein a current limiting element is insertd in a connection between the collector of said level converting transistor and the base of said driving transistor.

The current limiting element may be a resistor or, preferably, a diode.

The invention is illustrated in and further explained in connection with the accompanying drawings, in which: —

Figures 1*a* and 1*b* are diagrammatic sectional representations of the basic constructions of an SITL semi-conductor device and an IIL semi-conductor device, respectively;

Figures 2*a* and 2*b* are basic diagrammatic sectional representations of an SITL semiconductor device and an IIL semi-conductor device, respectively, showing the respective lamination constructions which are used to provide the circuitry;

Figures 3*a* and 3*b* are circuit diagrams showing the conventional signal-level converting circuits of an SITL semi-conductor device and an IIL semi-conductor device, respectively;

Figures 4*a* and 4*b* are circuit diagrams showing embodiments of the present invention, the former using an SITL semi-conductor device and the latter using an IIL semi-conductod device; and

Figures 5*a* and 5*b* are circuit diagrams showing further embodiments of the invention using an SITL semi-conductor device and an IIL semi-conductor device, respectively.

Referring to Figures 1*a* and 1*b*, these are respectively diagrammatic sectional views of the basic construction of an SITL semi-conductor device and of an IIL semiconductor device, with the different diffused portions represented in conventional manner, and identified by references applied to their terminals. In Figure 1*a* 101 is the emitter of an injector, 102*a* is the drain and 103*a* is the gate of a vertical field effect driving transistor X, and 104*a* is the base of the injector and the source of the driving transistor X. In Figure 1*b* 101 is the emitter of an injector, 102*b* is the collector and 103*b* is the base of a vertical NPN driving transistor Y, and 104*b* is the base of the injector and the emitter of the driving transistor Y.

Figures 2*a* and 2*b* are respectively diagrammatic sectional views showing the basic laminar circuit constructions of an SITL and of an IIL semi-conductor device. In Figure 2*a* 201 is an injector emitter, 202*a* is the drain, and 203*a* is the gate of a driving transistor X_1, 204 is the emitter of the injector, 205*a* is the drain, and 206*a* is the gate of a driving transistor X_2, 207*a* is the base of the injector and the source of said transistor X_2, and 208 is an isolation layer. In Figure 2*b* 201 is an injector emitter, 202*b* is the collector and 203*b* is the base of a driving transistor Y_1, 204 is the emitter of the injector, 205*b* is the collector and 206*b* is the base of the driving transister Y_2, and 207*b* is the base of the injector and the emitter of the driving transistor Y_2 and 208 is an isolation layer.

Figures 3*a* and 3*b* show respectively the circuit diagrams of conventional signal-level converting circuits with an SITL semi-conductor device and an IIL semiconductor device; Figures 4*a* and 4*b* show respectively the circuit diagrams of embodiments of this invention with an SITL semi-conductor device and an IIL semiconductor device; and Figures 5*a* and 5*b* respectively show the circuit diagrams of further embodiments of this invention with an SITL semi-conductor device and an IIL semi-conductor device.

In Figures 3*a* and 3*b*, for the SITL and the IIL cases, respectively, the circuitry is shown in a double-layer set-out, with the two layers indicated by the brackets 5 and 6. 1 is the positive power supply line which is connected to the positive terminal of a battery 2 (e.g. a battery of 1.5 volts) and 3 is the negative power supply line which is connected to the neagtive terminal of said battery. The upper-layer part 5 of the circuit is that above and the lower-layer part 6 of the circuti is that below, the connection line 4. The base current of transistor 7, which acts as the injector in the upper-layer part of the circuit, is supplied to a transistor 8, which acts as the injector in the lower-layer part circuit, *via* the connection line 4 so that effective use is made of the injection current from the battery.

The signal-level converting operation in the circuits of Figures 3*a* and 3*b* will now be described. To simplify the description, it is assumed that the battery voltage is 1.4 volts and the voltage on the connection line 4 is 0.7 volts, this being the base-emitter voltage of transistor 8. In other words, it is assumed that the uper-level part 5 of the circuit is operated with a logic amplitude from 0.7V to 1.4V and the lower-layer part 6 is operated with a logic amplitude from 0V to 0.7V.

In order to shorten the description, the operations of Figures 3*a* and 3*b* will be described together, references with *a* suffixes applying to Figure 3*a*, references with *b* suffixes applying to Figure 3*b* and references without letter suffixes applying to both figures.

When the voltage at an input terminal 10 is 1.4 volts, transistor 11*a* or 11*b* and level-converting transistor 12 are turned on. Therefore, transistor 13*a* or 13*b* in the lower-layer part 6 of the circuit is also turn on. At this time, since the collector current of the injector transistor 8 in the lower-layer part of the circuit goes to the transistor 13*a* or 13*b*, output transistor 14*a* or 14*b* will be turned off. Consequently, output terminal 16 will be at 0.7 volts due to the effect of the 0.7 volts drop set up across a constant current load provided by transistor 15.

On the other hand, if the voltage on the input terminal 10 is 0.7 volts, transistor 11*a* or 11*b* and the level-converting transistor 12 are turned off. Therefore, transistor 13*a* or 13*b* will be turned off. As a result, the collector current of the injector transistor 8 in the lower part 6 is injected to the gate of the output transistor 14*a* or to the base of the output transistor 14*b* and the output transistor 14*a* or 14*b* is turned on. The voltage at the output terminal 16 therefore becomes 0 volt. It will be seen, therefore, that, in both figures 3*a* and 3*b*, output becomes 0.7V when the input is 1.4V and 0V when the input is 0.7V, i.e. there is conversion of signal level.

Although the level-converting transistor 12 is turned on when the input signal voltage is 1.4 volts, at this time a voltage of 1.4 volts is applied to the gate of the transistor 13*a* or to the base of transistor 13*b* only if it is assumed that the collector-emitter saturation voltage $V_{CE\,Sat.}$ of the level-converting transistor 12 is sufficiently small in relation to 1.4 volts. Therefore, since a comparatively large current flows through the emitter of the level-converting transistor 12, the collector of said transistor 12, the gate of the transistor 13*a* (or the base of the transistor 13*b*) the source of the transistor 13*a* (or the emitter of the transistor 13*b*) there is still undesirably large power consumption in the respective laminar circuit constructions (Figures 2*a* and 2*b*) which provide effective use of injection current. This is a serious defect which it is the object of this invention to reduce or avoid.

Two embodiments of the invention, for the SITL and the IIL case respectively, are shown in Figures 4*a* and 4*b*. Comparing these figures with Figures 3*a* and 3*b* respectively, it will be seen that the difference lies in the insertion of a resistor 43 between the collector of the level-converting transistor 41 and the gate of the transistor 42*a* (Figure 4*a*) or the base of transistor 42*b* (Figure 4*b*). In the further embodiments, for the SITL and the IIL case respectively, shown in Figures 5*a* and 5*b*, a diode 44 replaces the resistor 43 of Figures 4*a* and 4*b*.

The embodiments of the invention shown in Figures 4*a*, 4*b*, 5*a* and 5*b* operate in essentially the same manner as has already been described in connection with Figures 3*a* and 3*b* and it is unnecessary, therefore, to repeat such description.

The value of the resistor 43 (Figues 4*a* and 4*b*) is so chosen that the collector current of the level-converting transistor 41 is not less than the necessary minimum gate current of the transistor 42*a* (in the case of Figulre 4*a*) or the necessary minimum base current of the transistor 42*b* (in the case of Figure 4*b*). The embodiments shown in Figures 5*a* and 5*b* have the advantage that the diode 44, integrated on the chip, occupies a smaller space than the resistor 43.

As will now be appreciated, the insertion, as described, of a resistor or of a diode, reduces current consumption without any adverse effect on the level-converting operation. The invention has therefore the advantage of providing a level-converting circuit semi-conductor device which is very suitable for use in apparatus in which operation over a long time by a battery of limited capacity is required—for example in an electronic battery-driven small timepiece, such as a wrist watch, in which an SITL or IIL device is employed as a logic semi-conductor level converting device. The invention, though of considerable advantage in such timepieces, is not limited to its application thereto.

WHAT WE CLAIM IS:—

1. A Static Induction Transistor Logic semi-conductor device having a lateral PNP transistor used as an injector and a vertical field effect transistor used as a driving transistor and constituting a signal level converting circuit of integrated laminated circuit construction on a chip and making use of injection current in said circuit, said circuit including a level converting transistor which converts a signal level from one part of the circuit to a different level in another part of the circuit wherein a current limiting element is inserted in a connection between the collector of said level converting transistor and the gate of the driving transistor.

2. An Integrated Injection Logic semiconductor device having a lateral PNP transistor used as an injector and a vertical NPN transistor used as a driving transistor and constituting a signal level converting circuit of integrated laminated circuit construction on a chip and making use of injection current in said circuit, said circuit including a level converting transistor which converts a signal level from one part of the circuit to a different level in another part of the circuit wherein a current limiting element is inserted in a con-

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2. An Integrated Injection Logic semiconductor device having a lateral PNP transistor used as an injector and a vertical NPN transistor used as a driving transistor and constituting a signal level converting circuit of integrated laminated circuit construction on a chip and making use of injection current in said circuit, said circuit including a level converting transistor which converts a signal level from one part of the circuit to a different level in another part of the circuit wherein a current limiting element is inserted in a con-

nection between the collector of said level converting transistor and the base of said driving transistor.

3. A device as claimed in claim 1 or 2 wherein said current limiting element is a resistor integrated on the chip.

4. A device as claimed in claim 1 or 2 wherein said current limiting element is a diode integrated on the chip.

5. A Static Induction Transistor Logic semi-conductor device substantially as herein described with reference to Figure 4*a* or 5*a* of the accompanying drawings.

6. An Integrated Injection Logic semi-conductor device substantially as hereby described with reference to Figure 4*b* or 5*b* of the accompanying drawings.

7. A battery operated electronic timepiece including a semi-conductor device as claimed in any of the preceding claims.

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Printed for Her Majesty's Stationery Office by The Tweeddale Press Ltd., Berwick-upon-Tweed, 1980.
Published at the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.