CLAIMS

1. An integrated circuit (IC) comprising:

a core logic having functional logic elements;

a wrapper chain having a plurality of flops for testing the core logic, wherein the plurality of flops of the wrapper chain are sequentially interconnected along a scan path for shifting scan data through successive ones of the flops during testing of the core logic; and

at least one state machine-driven flop connected along the scan path of the wrapper chain,

wherein the state machine-driven flop is individually configurable, during the testing, to output to the core logic a first value independent from the scan data being shifted along the scan path and received by the state machine-driven flop, and

wherein at least one flop of the plurality of flops is set to output to the core logic a second value that is equal to the scan data being shifted along the scan path and received by the at least one flop.

2. The IC of claim 1, wherein the state machine-driven flop is configurable, during testing, to maintain, as output, a current value of the state machine-driven flop that was shifted into the state machine-driven flop during a previous shift cycle of the wrapper chain.

3. The IC of claim 1, wherein the state machine-driven flop is configurable, during testing, to output an inverse of a current value of the state machine-driven flop that was shifted into the state machine-driven flop during a previous shift cycle of the wrapper chain.

4. The IC of claim 1, wherein the state machine-driven flop is configurable, during testing, to disable shifting of scan data into state machine-driven flop.

5. The IC of claim 1, wherein the wrapper chain comprises one of: (1) an input wrapper chain including a first plurality of flops to provide input data to test the core logic, or (2) an output wrapper chain including a second plurality of flops to receive output data from the core logic.

6. The IC of claim 1, wherein a connection between the state machine-driven flop and a previous flop in the wrapper chain propagates data to the state machine-driven flop at a rate less than an operational rate of the core logic.

7. The IC of claim 1, wherein the at least one state machine-driven flop is a first state machine-driven flop configured to output a current value of the first state machine-driven flop, wherein the IC further comprises a second state machine-driven flop configured to output an inverse of a current value of the second state machine-driven flop.

8. The IC of claim 1, wherein the state machine-driven flop comprises a first flip-flop and a second flip-flop, wherein a value shifted in the first flip-flop is a current value of the state machine-driven flop, and a value shifted in the second flip-flop configures the state machine-driven flop to output the current value of the state machine-driven flop or an inverse of the current value of the state machine-driven flop.

9. The IC of claim 8, wherein the state machine-driven flop is configured to:

load a first data bit of an input string of data during a load phase to the first flip-flop, wherein the first data bit represents a local data bit,

load a second data bit of the input string of data during the load phase to the second flip-flop, wherein the second data bit represents a toggle state data bit which indicates whether the state machine-driven flop is in a toggle mode or in a maintain mode,

wherein when the state machine-driven flop is in the maintain mode, the state machine-driven flop outputs a current value of the local data bit, and

wherein when the state machine-driven flop is in the toggle mode, the state machine-driven flop outputs the inverse of the current value of the local data bit.

10. The IC of claim 1, wherein during a load phase of the testing, the plurality of flops and the state machine-driven flop are configured to load data bits received from connections with respective flops, in response to a clock signal having a first frequency, and wherein during a capture phase of the testing, the state machine-driven flop is configured to output the

value independent from the scan data being shifted, in response to the clock signal having a second frequency that is greater than the first frequency.

11. The IC of claim 1, wherein the state machine-driven flop includes a next state logic gate including a first next state logic gate input, a second next state logic gate input, and a next state logic gate output.

12. The IC of claim 11, wherein when the state machine-driven flop is operating in a toggle mode to output an inverse of a current value, the second flip-flop is configured to forward a toggle mode data bit value to the first next state logic gate input, and the next state logic gate is configured to toggle, in response to receiving the toggle mode data bit value, the current value to the inverse of the current value.

13. The IC of claim 11, wherein when the state machine-driven flop is operating in a maintain mode to output a current value, the second flip-flop is configured to forward a maintain mode data bit value to the first next state logic gate input, and the next state logic gate is configured to maintain, in response to receiving the maintain mode data bit value at the first next state logic gate input, the current value.

14. The IC of claim 1,

wherein the wrapper chain comprises an input wrapper chain, and wherein the IC further includes an output wrapper chain,

wherein the input wrapper chain is configured to:

load, during a load phase responsive to receiving a set of load phase clock signals at a slow clock frequency, an input string of data from a tester,

wherein the output wrapper chain is configured to:

capture, during a capture phase responsive to receiving a set of capture phase clock signals at a fast clock frequency, a captured string of data from a plurality of functional paths through the core logic; and

unload, during an unload phase responsive to receiving a set of unload phase clock signals at the slow clock frequency, the captured string of data to the tester.

15. A system comprising:

a tester; and

an integrated circuit (IC) comprising:

a core logic having functional logic elements;

an input wrapper chain having a plurality of flops for testing the core logic, wherein the plurality of flops of the wrapper chain are sequentially interconnected along a scan path for shifting scan data through successive ones of the flops during testing of the core logic;

an output wrapper chain; and

at least one state machine-driven flop connected along the scan path of the input wrapper chain, wherein the state machine-driven flop is individually configurable, during the testing, to output a value independent from the scan data being shifted along the scan path and received by the state machine-driven flop;

wherein the input wrapper chain is configured to:

load, during a load phase responsive to receiving a set of load phase clock signals at a slow clock frequency, an input string of data from the tester so as to load values into the plurality of flops and configure the state machine-driven flop to output the value independent from the scan data being shifted along the scan path;

wherein the output wrapper chain is configured to:

capture, during a capture phase responsive to receiving a set of capture phase clock signals at a fast clock frequency, a captured string of data from a plurality of functional paths through the core logic; and

unload, during an unload phase responsive to receiving a set of unload phase clock signals at the slow clock frequency, the captured string of data to the tester.

16. The system of claim 15, wherein the tester is configured to:

compare the captured string of data with an expected string of data, wherein the expected string of data represents data which the core logic is expected to generate based on the input string of data; and

determine, based on the comparison, whether the plurality of functional paths perform one or more errors in generating the captured string of data.

17. The system of claim 15, wherein the state machine-driven flop is configurable, during testing, to maintain, as output, a current value of the state machine-driven flop that was shifted into the state machine-driven flop during a previous shift cycle of the wrapper chain.

18. The system of claim 15, wherein the state machine-driven flop is configurable, during testing, to output an inverse of a current value of the state machine-driven flop that was shifted into the state machine-driven flop during a previous shift cycle of the wrapper chain.

19. The system of claim 15, wherein the state machine-driven flop is configurable, during testing, to disable shifting of scan data into state machine-driven flop.

20. The system of claim 15, wherein the state machine-driven flop comprises a first flip-flop and a second flip-flop, wherein a value shifted in the first flip-flop is a current value of the state machine-driven flop, and a value shifted in the second flip-flop configures the state machine-driven flop to output the current value of the state machine-driven flop or an inverse of the current value of the state machine-driven flop.