CLAIMS

1. A method for demoting data from a cache comprising heterogeneous memory types, the method comprising:

maintaining, for a data element, a write access count that is incremented each time a data element is updated in a cache, the cache comprising a higher performance portion and a lower performance portion;

storing the data element in both the higher performance portion and the lower performance portion;

removing the data element from the higher performance portion in accordance with a cache demotion algorithm;

upon removing the data element from the higher performance portion, determining if the data element also resides in the lower performance portion and the write access count is below a first threshold and, if so, ;

in response to removing the data element from the higher performance portion and determining that the write access count is below the first threshold, leaving the data element in the lower performance portion; and

determining if the data element also resides in response to removing the lowerdata element from the higher performance portion and determining that the write access count is at or above the first threshold and, if so, removing the data element from the lower performance portion.

2. The method of claim 1, further comprising if, upon removing the data element from the higher performance portion, the data element does not also reside in the lower performance portion, a write access count associated with the data element is below the first threshold, and a read access count associated with the data element is above a second threshold, placing the data element in the lower performance portion. .

3. The method of claim 2, further comprising only placing the data element in the lower performance portion if the data element is not a sequential data element.

4. 2. The method of claim 1, wherein the data element is a track.

~~5.~~ 3. The method of claim 1, wherein removing the data element from the higher performance portion comprises removing the data element from the higher performance portion when the higher performance portion is full.

~~6.~~ 4. The method of claim 1, wherein the higher performance portion is made up of dynamic random access memory (DRAM) and the lower performance portion is made up of storage class memory (SCM).

~~7.~~ 5. The method of claim 1, wherein the lower performance portion has a larger storage capacity than the higher performance portion.

~~8.~~ 6. A computer program product for demoting data from a cache comprising heterogeneous memory types, the computer program product comprising a non-transitory computer-readable storage medium having computer-usable program code embodied therein, the computer-usable program code configured to perform the following when executed by at least one processor:

~~maintain~~, for a data element, a write access count that is incremented each time a data element is updated in a cache, the cache comprising a higher performance portion and a lower performance portion;

~~store~~ the data element in both the higher performance portion and the lower performance portion;

remove the data element from the higher performance portion in accordance with a cache demotion algorithm;

~~upon~~ removing the data element from the higher performance portion, determine if the ~~data element also resides in the lower performance portion and the~~ write access count is below a first threshold ~~and, if so,~~ ;

in response to removing the data element from the higher performance portion and determining that the write access count is below the first threshold, leave the data element in the lower performance portion; and

~~determine if the data element also resides~~ in response to removing the ~~lower~~data element from the higher performance portion and determining that the write access count is at or above the first threshold ~~and, if so~~, remove the data element from the lower performance portion.

~~9. The computer program product of claim 8, wherein the computer-usable program code is further configured to if, upon removing the data element from the higher performance portion, the data element~~

~~does not also reside in the lower performance portion, a write access count associated with the data element is below the first threshold, and a read access count associated with the data element is above a second threshold, placing the data element in the lower performance portion.~~

~~10.~~ 7. The computer program product of claim 6, wherein the data element is a track.

8. The computer program product of claim ~~9, wherein the computer-usable program code is further configured to only place the data element in the lower performance portion if the data element is not a sequential data element.~~

~~11. The computer program product of claim 8, wherein the data element is a track.~~

~~12. The computer program product of claim 8~~6, wherein removing the data element from the higher performance portion comprises removing the data element from the higher performance portion when the higher performance portion is full.

~~13.~~ 9. The computer program product of claim ~~8~~6, wherein the higher performance portion is made up of dynamic random access memory (DRAM) and the lower performance portion is made up of storage class memory (SCM).

~~14.~~ 10. The computer program product of claim ~~8~~6, wherein the lower performance portion has a larger storage capacity than the higher performance portion.

~~15.~~ 11. A system for demoting data from a cache comprising heterogeneous memory types, the system comprising:

~~at least one processor; and~~

~~at least one memory device operably coupled to the at least one processor and storing instructions for execution on the at least one processor, the instructions causing the at least one processor to:~~

~~maintain, for a data element, a write access count that is incremented each time a data element is updated in a cache, the cache comprising a higher performance portion and a lower performance portion;~~

store the data element in both the higher performance portion and the lower performance portion;

remove the data element from the higher performance portion in accordance with a cache demotion algorithm;

upon removing the data element from the higher performance portion, determine if the data element also resides in the lower performance portion and the write access count is below a first threshold and, if so, ;

in response to removing the data element from the higher performance portion and determining that the write access count is below the first threshold, leave the data element in the lower performance portion; and

determine if the data element also resides in response to removing the lowerdata element from the higher performance portion and determining that the write access count is at or above the first threshold and, if so, remove the data element from the lower performance portion.

16. The system of claim 15, wherein the instructions further cause the at least one processor to if, upon removing the data element from the higher performance portion, the data element does not also reside in the lower performance portion, a write access count associated with the data element is below the first threshold, and a read access count associated with the data element is above a second threshold, placing the data element in the lower performance portion.

17. The system of claim 16, wherein the instructions further cause the at least one processor to only place the data element in the lower performance portion if the data element is not a sequential data element.

18. The system of claim 1512. The system of claim 11, wherein removing the data element from the higher performance portion comprises removing the data element from the higher performance portion when the higher performance portion is full.

19. 13. The system of claim 1511, wherein the higher performance portion is made up of dynamic random access memory (DRAM) and the lower performance portion is made up of storage class memory (SCM).

~~20.~~ 14. The system of claim ~~15~~11, wherein the lower performance portion has a larger storage capacity than the higher performance portion.