CLAIMS

1. A clock generation circuit, comprising:

an oscillation circuit, configured to generate a first oscillation signal and a second oscillation signal, wherein a frequency of the first oscillation signal is same as a frequency of the second oscillation signal, and a phase of the first oscillation signal is opposite to a phase of the second oscillation signal;

a comparison unit, configured to receive the first oscillation signal and the second oscillation signal, and compare at least one of: a duty cycle of the first oscillation signal or a duty cycle of the second oscillation signal; and

a logical unit, connected to the comparison unit and the oscillation circuit, and configured to control the oscillation circuit according to an output result of the comparison unit, so that the duty cycles reach a preset range;

wherein the comparison unit comprises:

an integral unit, having a first input end for receiving one of the first oscillation signal or the second oscillation signal, and a second input end for receiving another one of the second oscillation signal or the first oscillation signal; and

a comparator, connected to an output end of the integral unit;

wherein the integral unit is configured such that:

the first input end of the integral unit receives the first oscillation signal when a turnover identification signal is at a low level, and receives the second oscillation signal when the turnover identification signal is at a high level; and

the second input end of the integral unit receives the second oscillation signal when the turnover identification signal is at a low level, and receives the first oscillation signal when the turnover identification signal is at a high level;

wherein the logical unit comprises:

a counter, configured to adjust at least one of the duty cycle of the first oscillation signal or the duty cycle of the second oscillation signal;

a first register group, configured to store a first value of the counter corresponding to an output of the comparator having one inversion point when the turnover identification signal is at a low level; and

a second register group, configured to store a second value of the counter corresponding to the output of the comparator having the inversion point when the turnover identification signal is at a high level.

2. The clock generation circuit of claim 1, wherein the logical unit further comprises:

an operation component, connected to the first register group and the second register group, and configured to perform at least one operation of addition, subtraction, multiplication or division on outputs of the first register group and the second register group; and

a third register group, connected to the operation component, and configured to store an output result of the operation component.

3. The clock generation circuit of claim 2, wherein the comparison unit is driven by a sampling clock, and a frequency of the sampling clock is lower than the frequency of the first oscillation signal and/or the frequency of the second oscillation signal.

4. The clock generation circuit of claim 3, wherein the counter is driven by a calculator clock, and a frequency of the calculator clock is lower than the frequency of the first oscillation signal and/or the frequency of the second oscillation signal.

5. The clock generation circuit of claim 4, wherein the frequency of the sampling clock is same as the frequency of the calculator clock.

6. The clock generation circuit of claim 5, further comprising:

a frequency divider, configured to receive an external clock signal, and generate the sampling clock and the calculator clock.

7. The clock generation circuit of claim 6, further comprising:

a fifth register group, connected with the frequency divider, and configured to configure the frequency of the sampling clock and the frequency of the calculator clock.

8. The clock generation circuit of claim 1, wherein the oscillation circuit comprises:

an oscillator, configured to generate a first initial oscillation signal and a second initial oscillation signal, wherein a frequency of the first initial oscillation signal is same as a frequency of the second initial oscillation signal, and a phase of the first initial oscillation signal is opposite to a phase of the second initial oscillation signal; and

a path simulation circuit, located between the oscillator and the comparison unit, wherein one end of the path simulation circuit is connected to an output end of the oscillator, another end of the path simulation circuit is connected to an input end of the comparison unit, and the path simulation circuit is configured to simulate circuit characteristics of a first path, generate the first oscillation signal by receiving the first initial oscillation signal, and generate the second oscillation signal by receiving the second initial oscillation signal.

9. The clock generation circuit of claim 8, further comprising:

a fourth register group, connected with the oscillator, and configured to configure the frequency of the first oscillation signal and the frequency of the second oscillation signal.

10. The clock generation circuit of claim 9, further comprising:

a sixth register group, connected with the path simulation circuit, and configured to configure electrical parameters of the path simulation circuit.

11. A memory, comprising:

the clock generation circuit of any one of claims 1-10.

12. A method for calibrating a clock duty cycle, comprising:

generating, by an oscillation circuit, a first oscillation signal and a second oscillation signal, wherein a frequency of the first oscillation signal is same as a frequency of the second oscillation signal, and a phase of the first oscillation signal is opposite to a phase of the second oscillation signal, and the first oscillation signal having an initial duty cycle;

receiving, by a comparison unit, the first oscillation signal and the second oscillation signal, and comparing a duty cycle of the first oscillation signal or a duty cycle of the second oscillation signal; and

controlling, by a logical unit, the oscillation circuit according to an output result of the comparison unit, so that the duty cycle of the first oscillation signal generated by the oscillation circuit changes from the initial duty cycle to a preset duty cycle;

wherein receiving, by the comparison unit, the first oscillation signal and the second oscillation signal comprising:

comparing, by the comparison unit, the duty cycle of the first oscillation signal when a turnover identification signal is at a low level; and

comparing, by the comparison unit, the duty cycle of the second oscillation signal when the turnover identification signal is at a high level;

wherein controlling, by the logical unit, the oscillation circuit according to the output result of the comparison unit comprising that:

the logical unit comprises a counter, a first register group and a second register group;

when the turnover identification signal is at a low level, the counter counts from M to N, when a value of the counter is M, the duty cycle of the first oscillation signal is P%, when a value of the counter is N, the duty cycle of the first oscillation signal is Q%, and when an output result of the comparison unit changes from low level to high level, a counter value corresponding to the counter at this time is stored in the first register group; and

when the turnover identification signal is at a high level, the counter counts from M to N, when a value of the counter is M, the duty cycle of the second oscillation signal is Q%, when a value of the counter is N, the duty cycle of the second oscillation signal is P%, and when the output result of the comparison unit changes from high level to low level, a counter value corresponding to the counter at this time is stored in the second register group;

wherein both M and N are integers, M is less than N, both P and Q are positive integers, P is less than 50, and Q is greater than 50.

13. The method for calibrating the clock duty cycle of claim 12, wherein controlling, by the logical unit, the oscillation circuit according to the output result of the comparison unit, comprising that:

the logical unit further comprises an operation component and a third register group;

the operation component performs at least one operation of addition, subtraction, multiplication or division on outputs of the first register group and the second register group, and stores an obtained value L in the third register group;

wherein the L is a positive integer, and L is greater than or equal to M and less than or equal to N.

14. The method for calibrating the clock duty cycle of claim 13, wherein the duty cycle of the first oscillation signal corresponding to the L is the preset duty cycle.