10

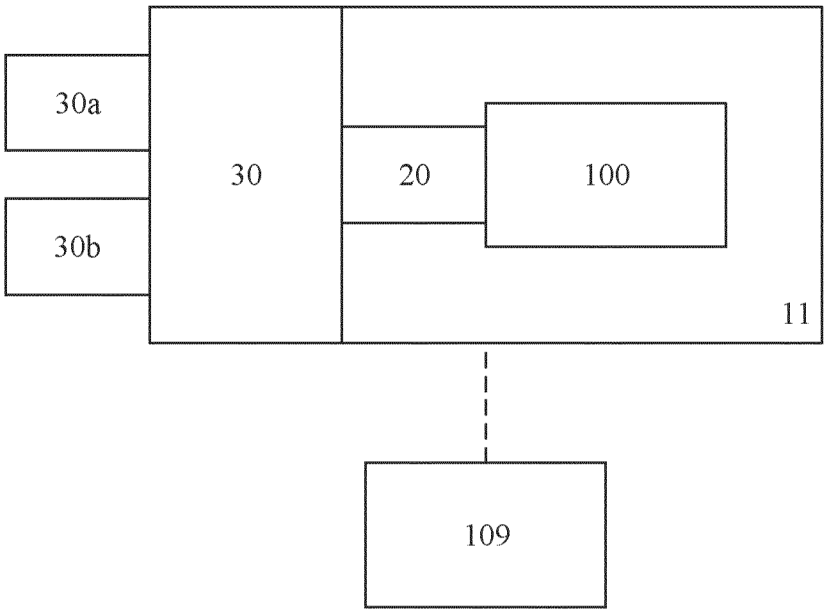


FIG. 1

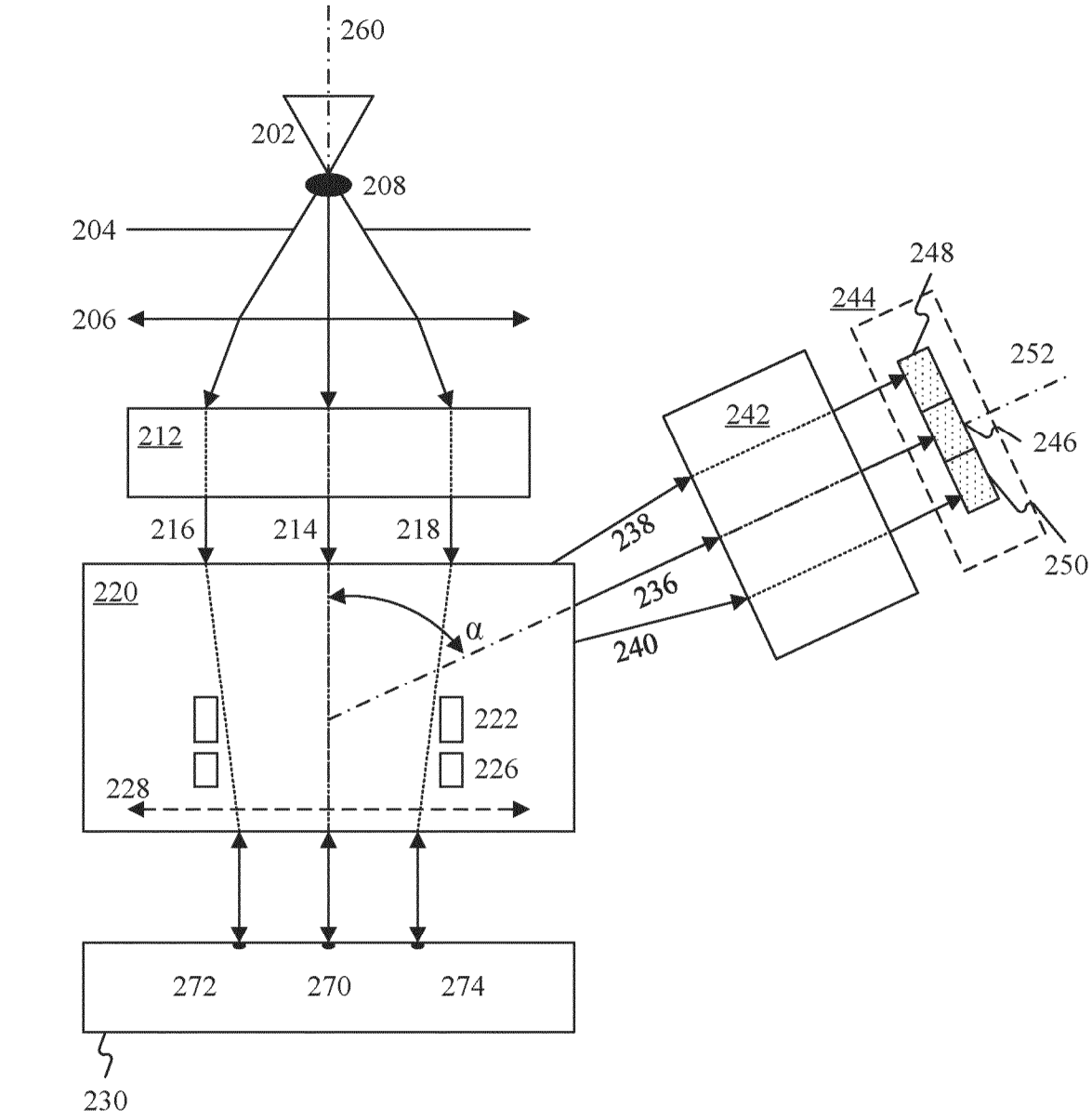

100A
260
202
208
204
206
212
216
214
218
220
α
222
226
228
272
270
274
230
238
236
240
242
244
248
252
246
250

FIG. 2A

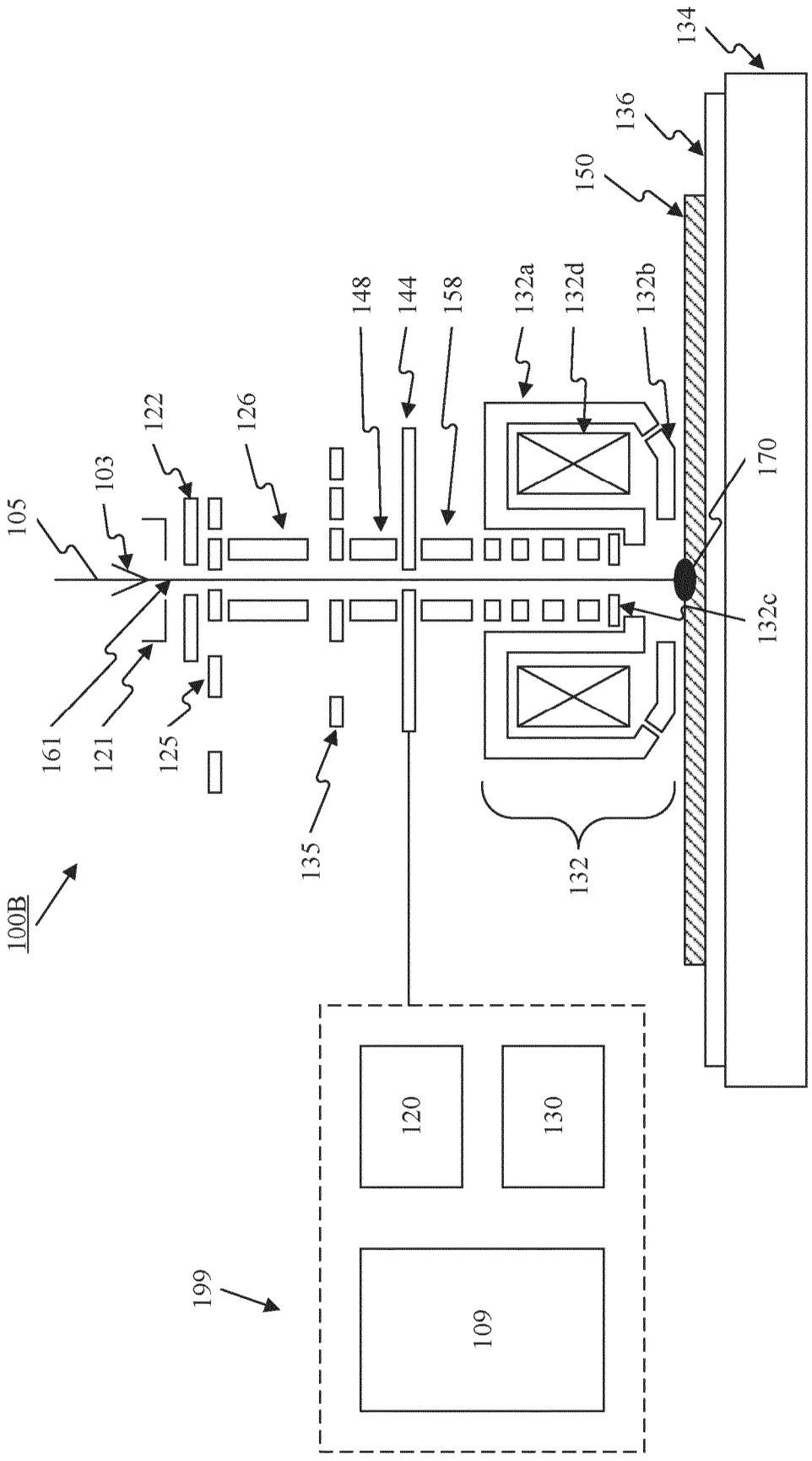

100B
105
103
122
126
148
144
158
132a
132d
132b
134
136
150
170
161
121
125
135
132
132c
199
109
120
130

FIG. 2B

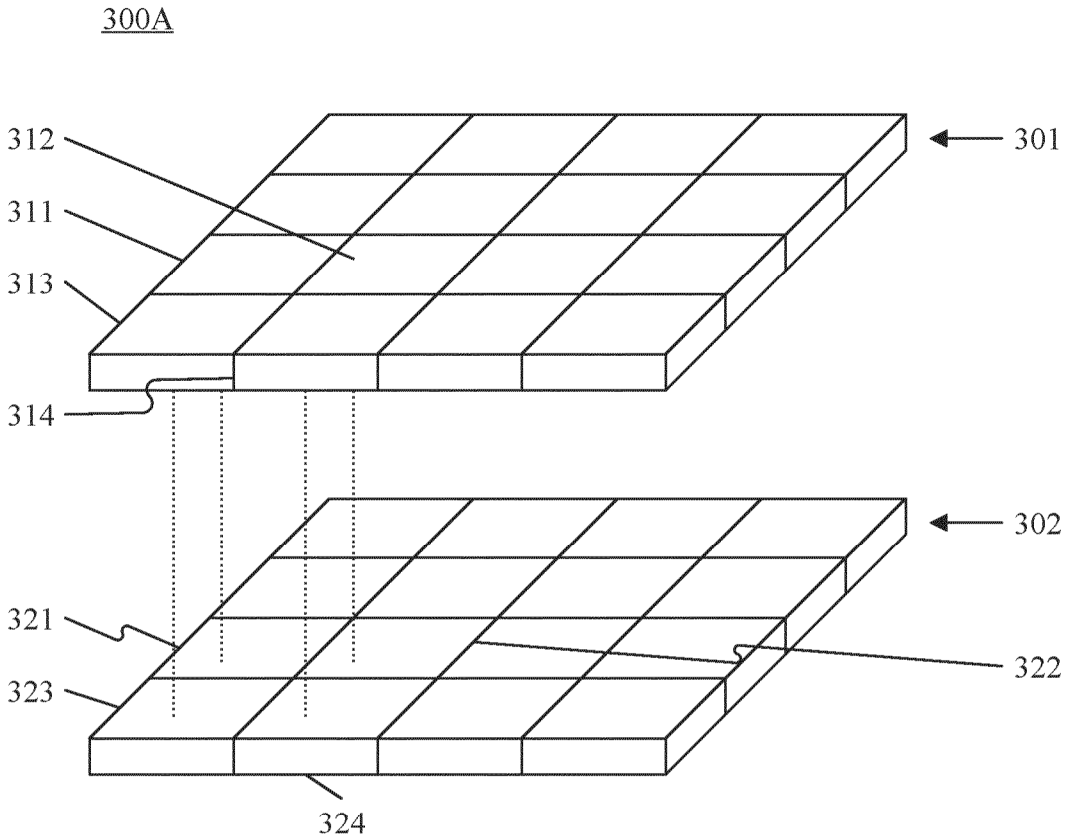

300A
312
311
313
314
301
302
321
323
322
324

FIG. 3A

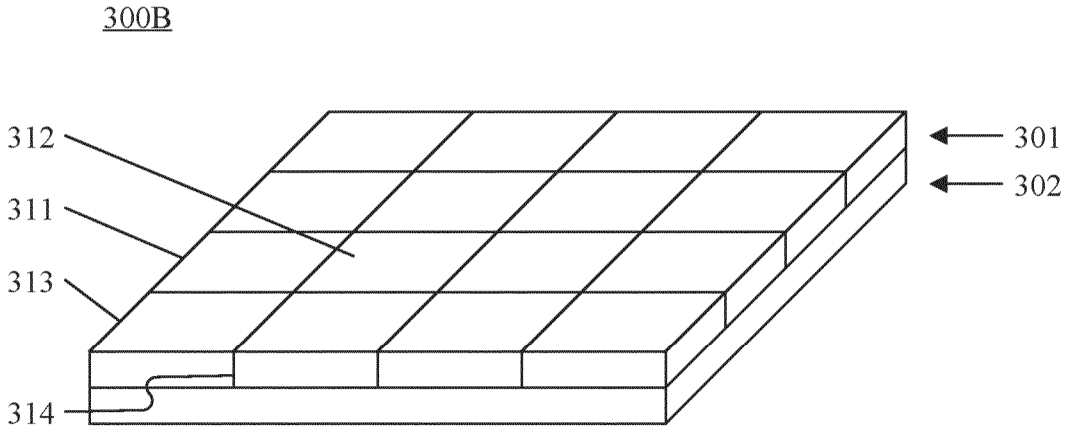

300B
312
311
313
314
301
302

FIG. 3B

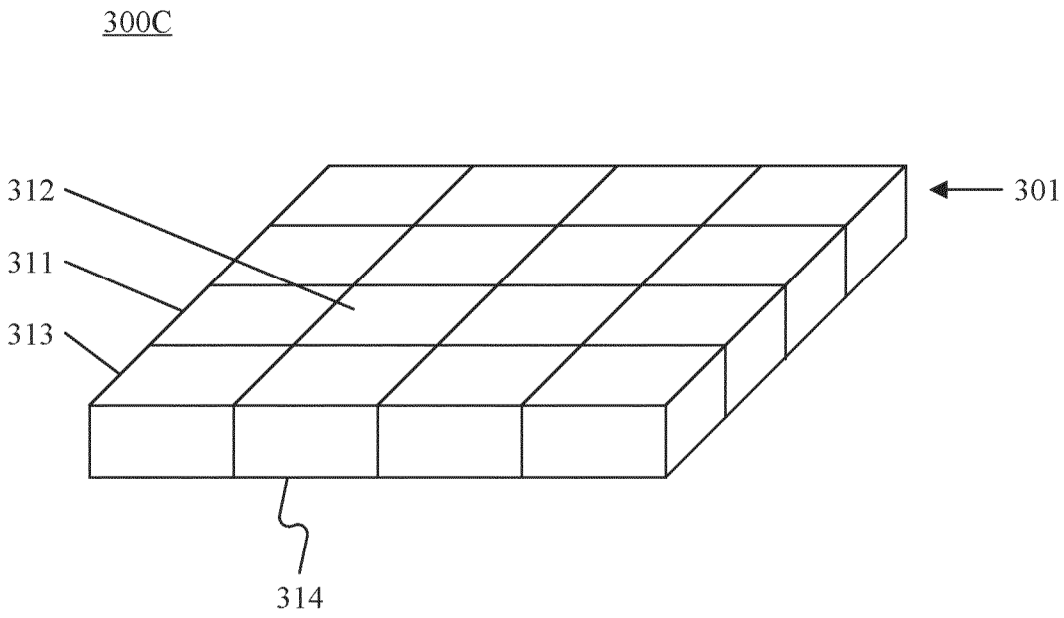


FIG. 3C

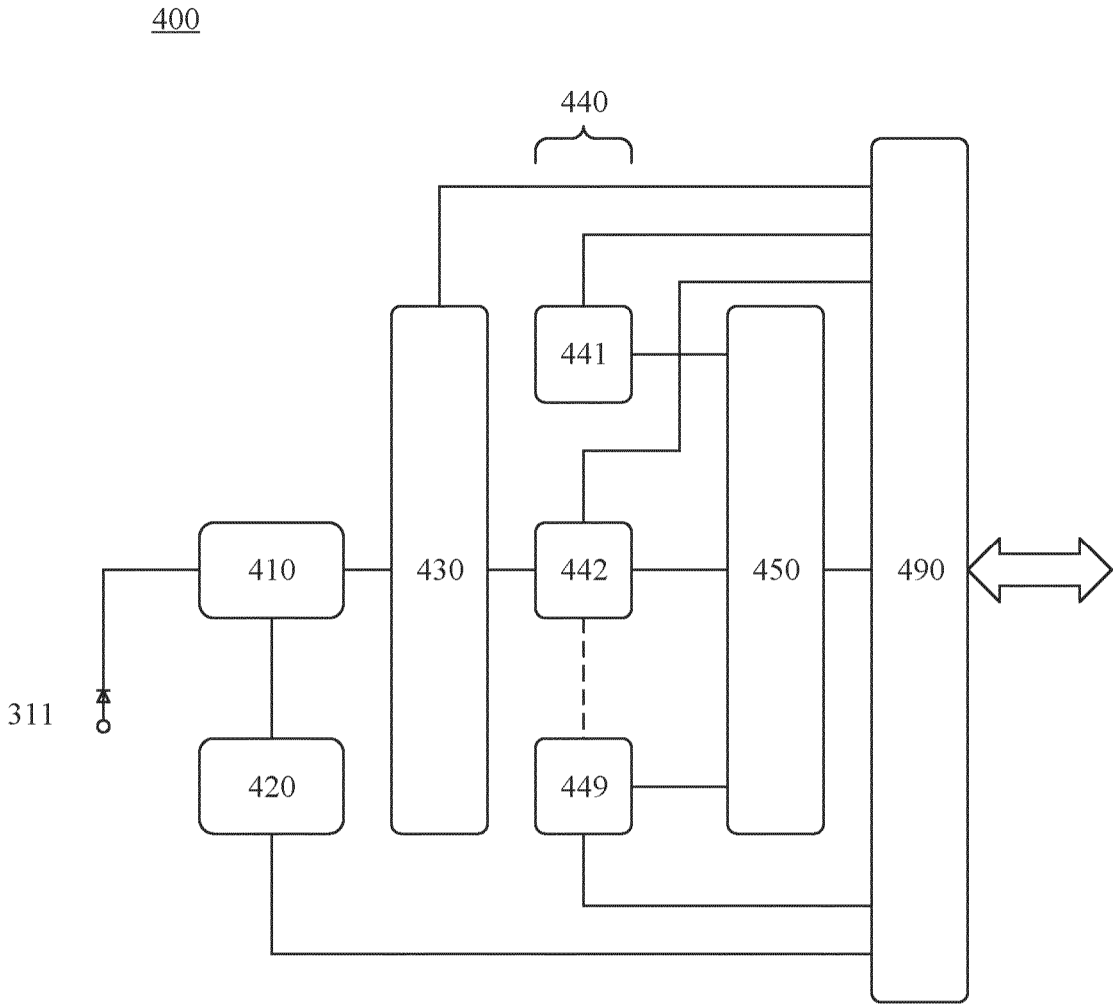


FIG. 4

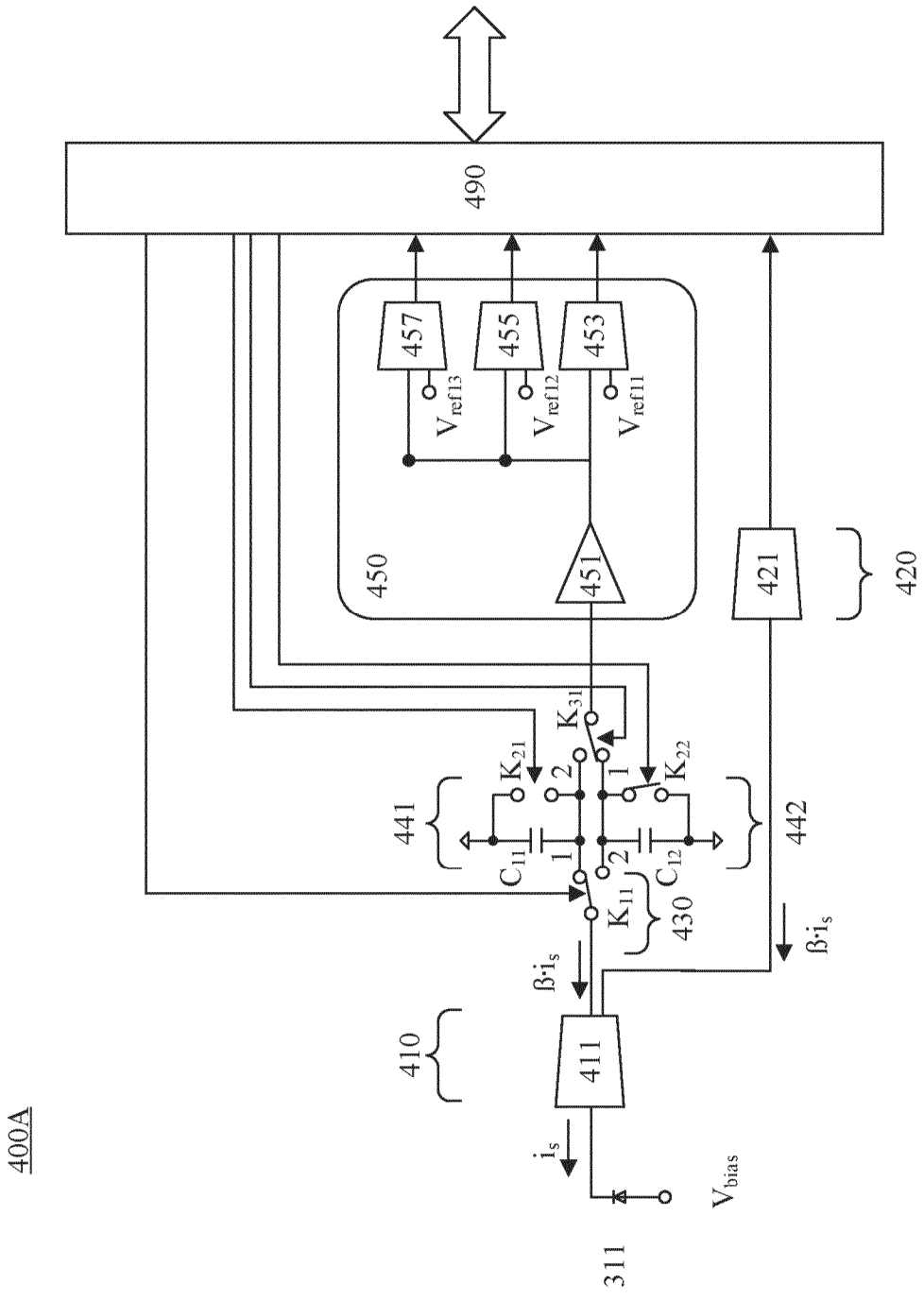

400A
490
457
455
453
V_{ref13}
V_{ref12}
V_{ref11}
450
451
421
420
K_{31}
K_{21}
K_{22}
441
442
C_{11}
C_{12}
K_{11}
430
$\beta \cdot i_s$
$\beta \cdot i_s$
410
411
i_s
V_{bias}
311

FIG. 5A

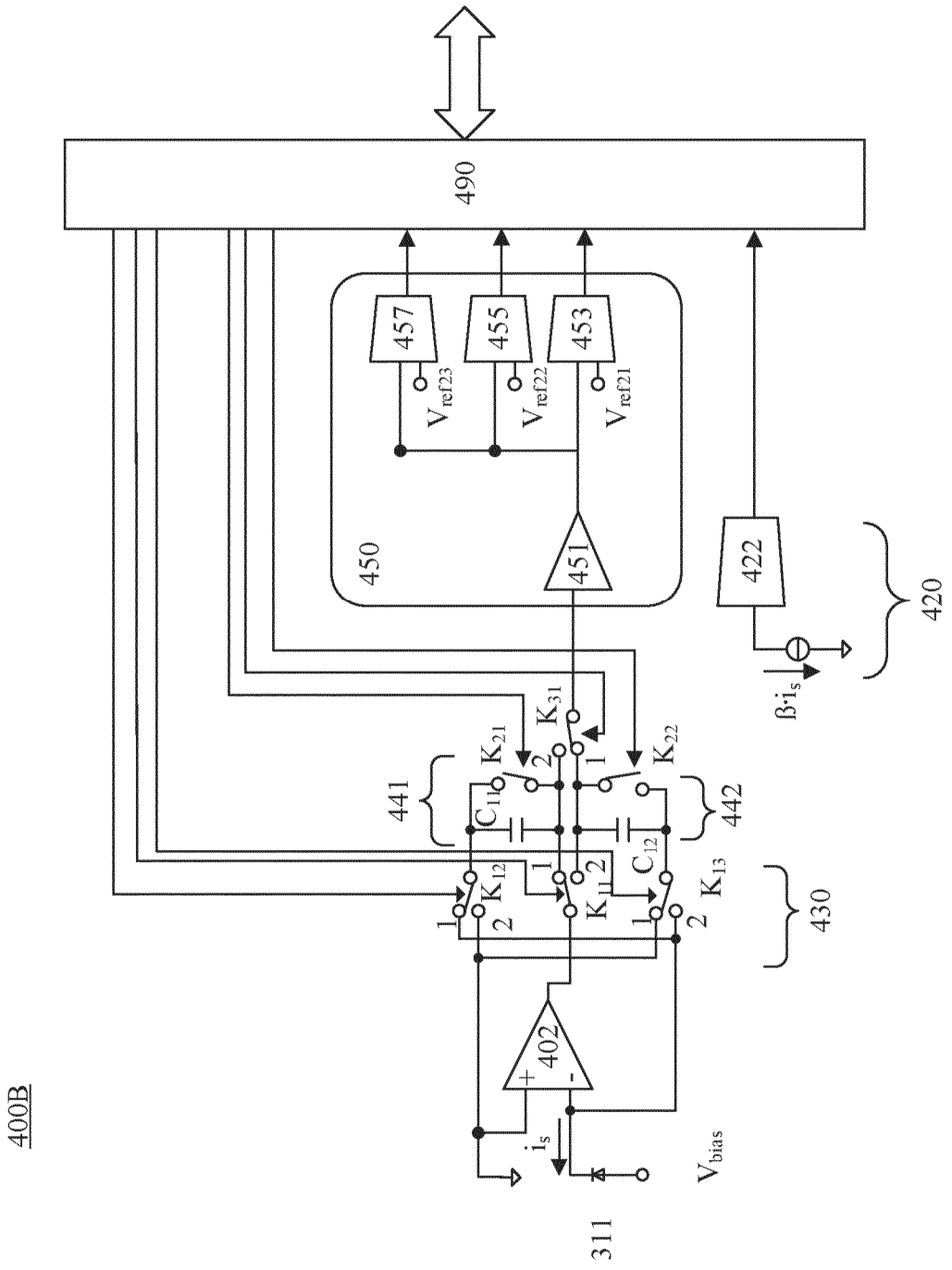

400B
490
457
455
453
V_{ref23}
V_{ref22}
V_{ref21}
450
451
422
420
$\beta \cdot i_s$
K_{21}
K_{31}
K_{22}
441
442
C_{11}
C_{12}
K_{12}
K_{11}
K_{13}
430
402
i_s
V_{bias}
311

FIG. 5B

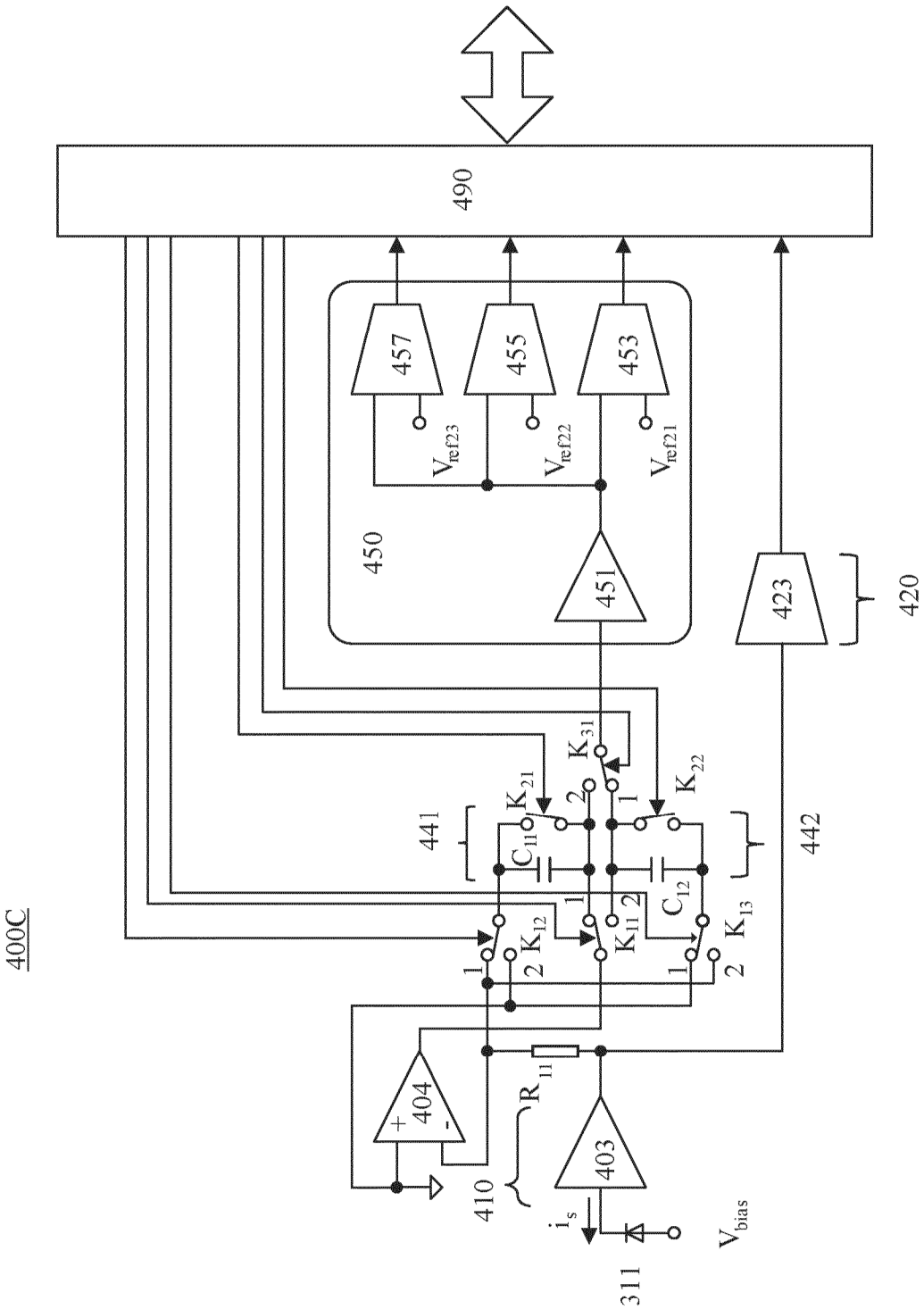

400C
490
457
455
453
450
V_{ref23}
V_{ref22}
V_{ref21}
451
423
420
441
442
K_{31}
K_{21}
K_{22}
K_{12}
K_{11}
K_{13}
C_{11}
C_{12}
404
R_{11}
403
410
i_s
311
V_{bias}

FIG. 5C

600

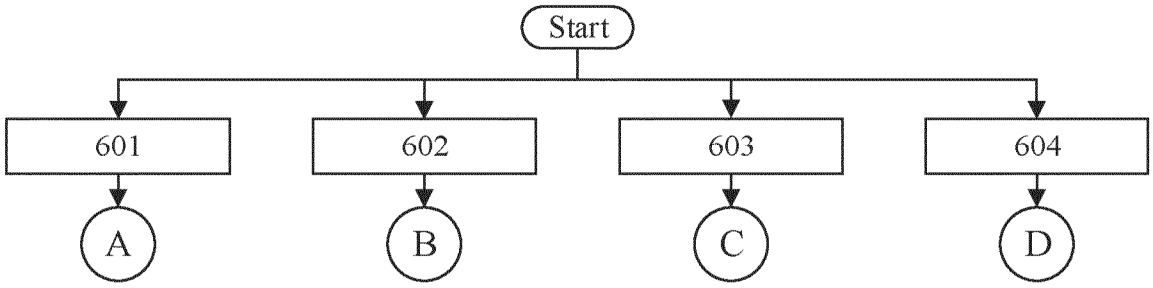


FIG. 6

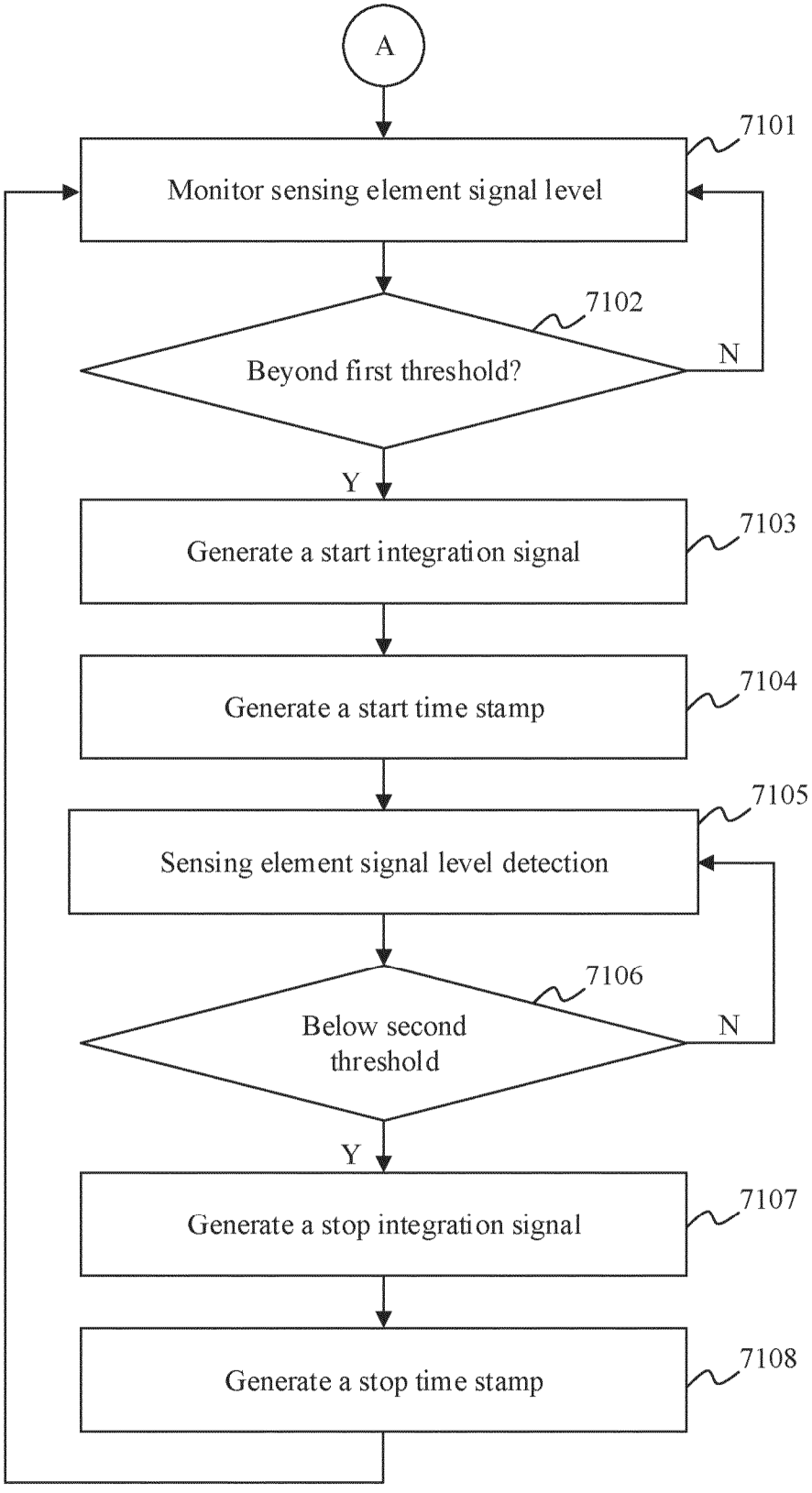

A
7101
Monitor sensing element signal level
7102
Beyond first threshold?
N
Y
7103
Generate a start integration signal
7104
Generate a start time stamp
7105
Sensing element signal level detection
7106
Below second threshold
N
Y
7107
Generate a stop integration signal
7108
Generate a stop time stamp

FIG. 7A

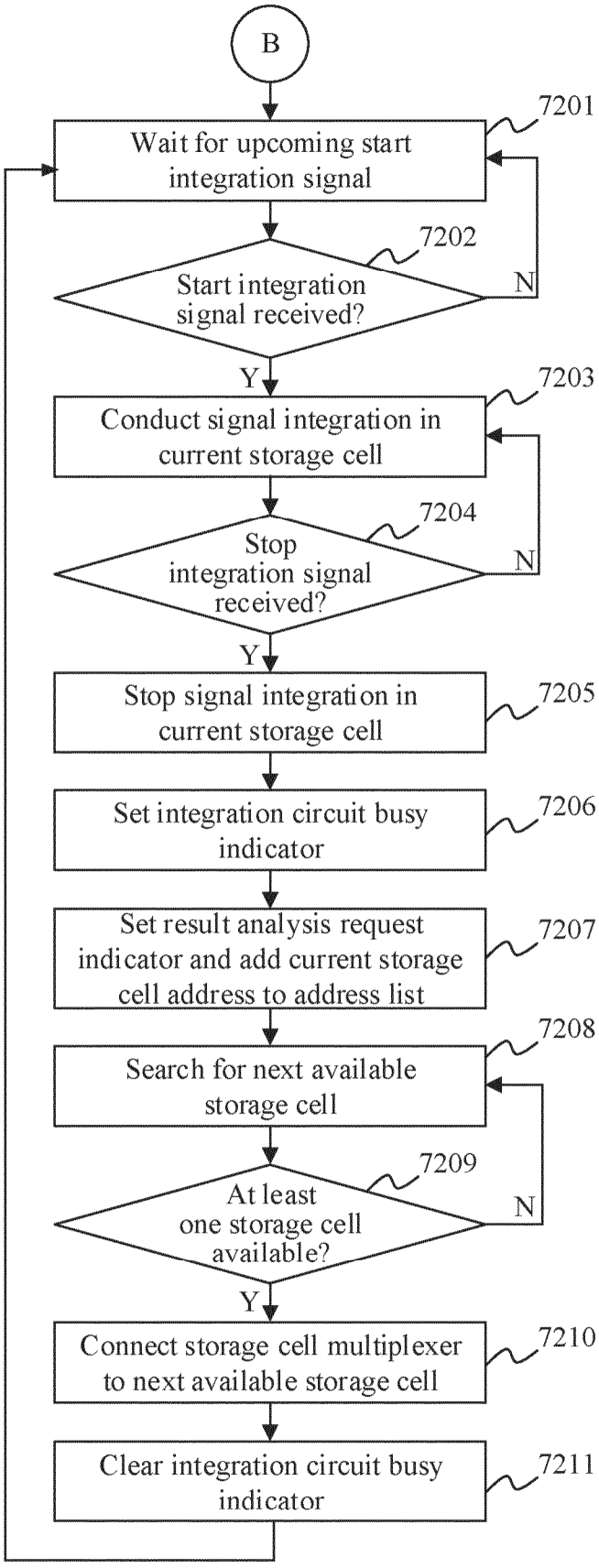

B
7201
Wait for upcoming start integration signal
7202
Start integration signal received?
N
Y
7203
Conduct signal integration in current storage cell
7204
Stop integration signal received?
N
Y
Stop signal integration in current storage cell
7205
Set integration circuit busy indicator
7206
Set result analysis request indicator and add current storage cell address to address list
7207
Search for next available storage cell
7208
7209
At least one storage cell available?
N
Y
Connect storage cell multiplexer to next available storage cell
7210
Clear integration circuit busy indicator
7211

FIG. 7B

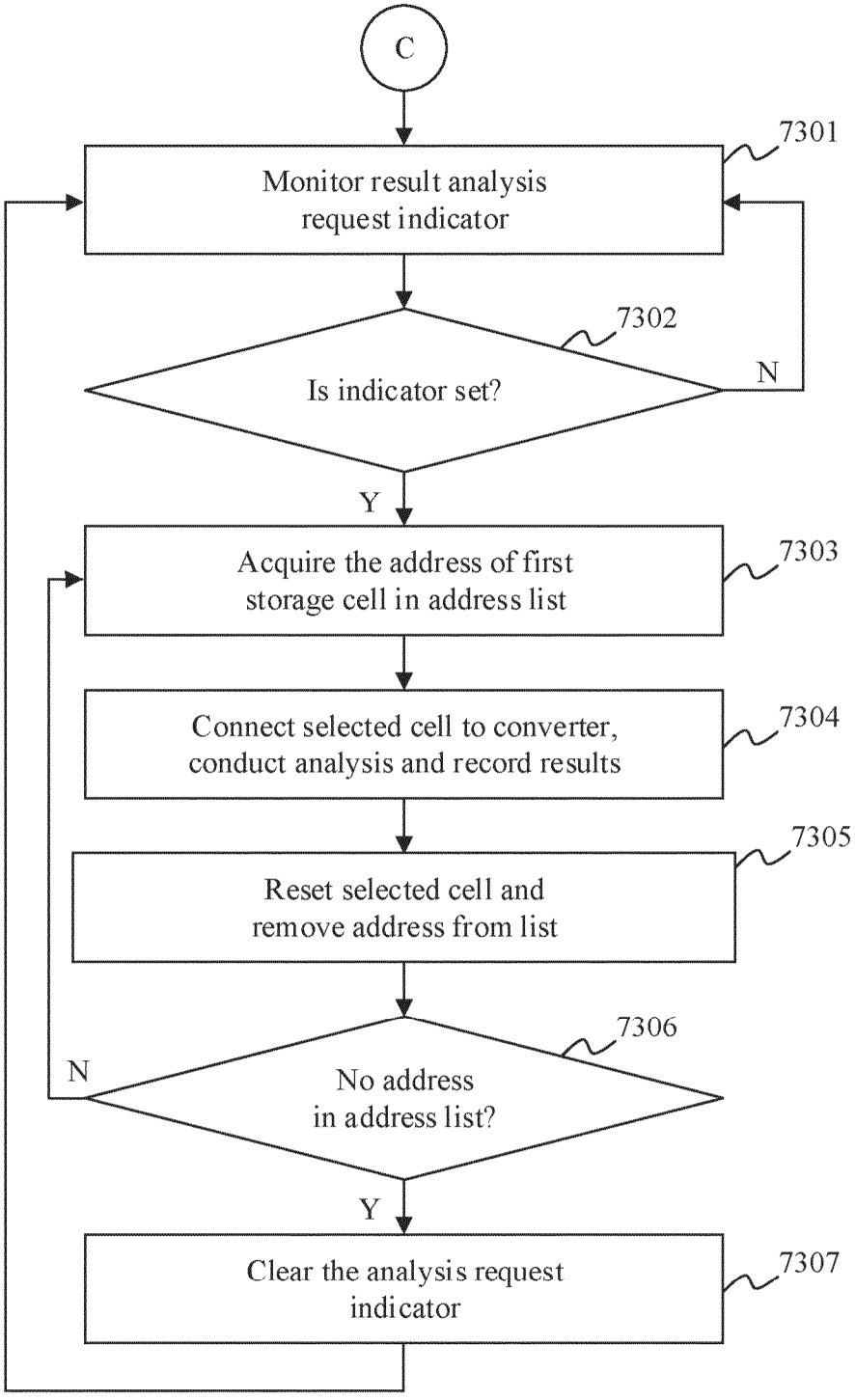

C
7301
Monitor result analysis request indicator
7302
Is indicator set?
N
Y
7303
Acquire the address of first storage cell in address list
7304
Connect selected cell to converter, conduct analysis and record results
7305
Reset selected cell and remove address from list
7306
N
No address in address list?
Y
7307
Clear the analysis request indicator

FIG. 7C

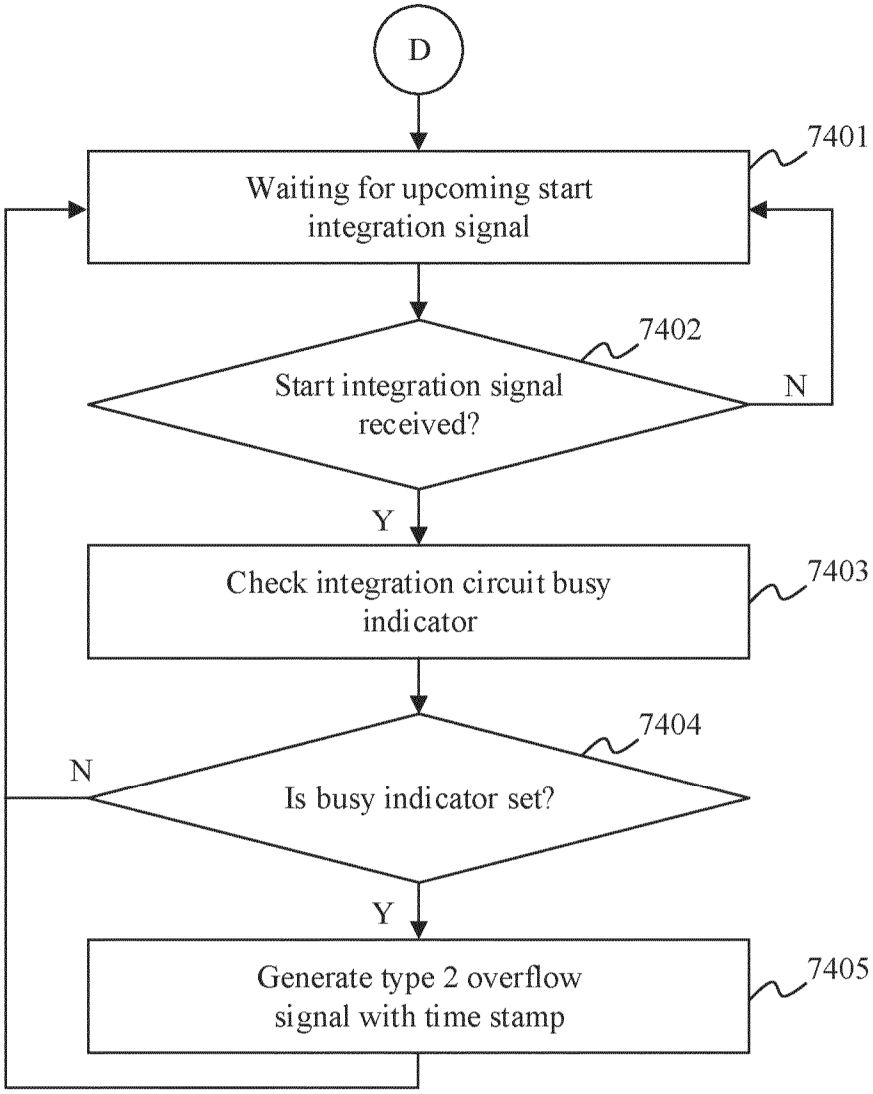

D
7401
Waiting for upcoming start integration signal
7402
Start integration signal received?
N
Y
7403
Check integration circuit busy indicator
7404
N
Is busy indicator set?
Y
7405
Generate type 2 overflow signal with time stamp

FIG. 7D

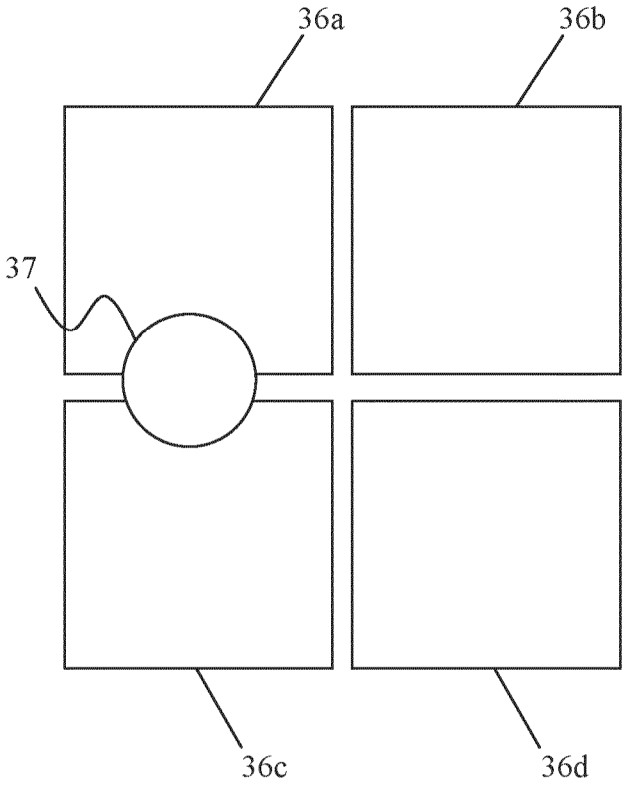


FIG. 8

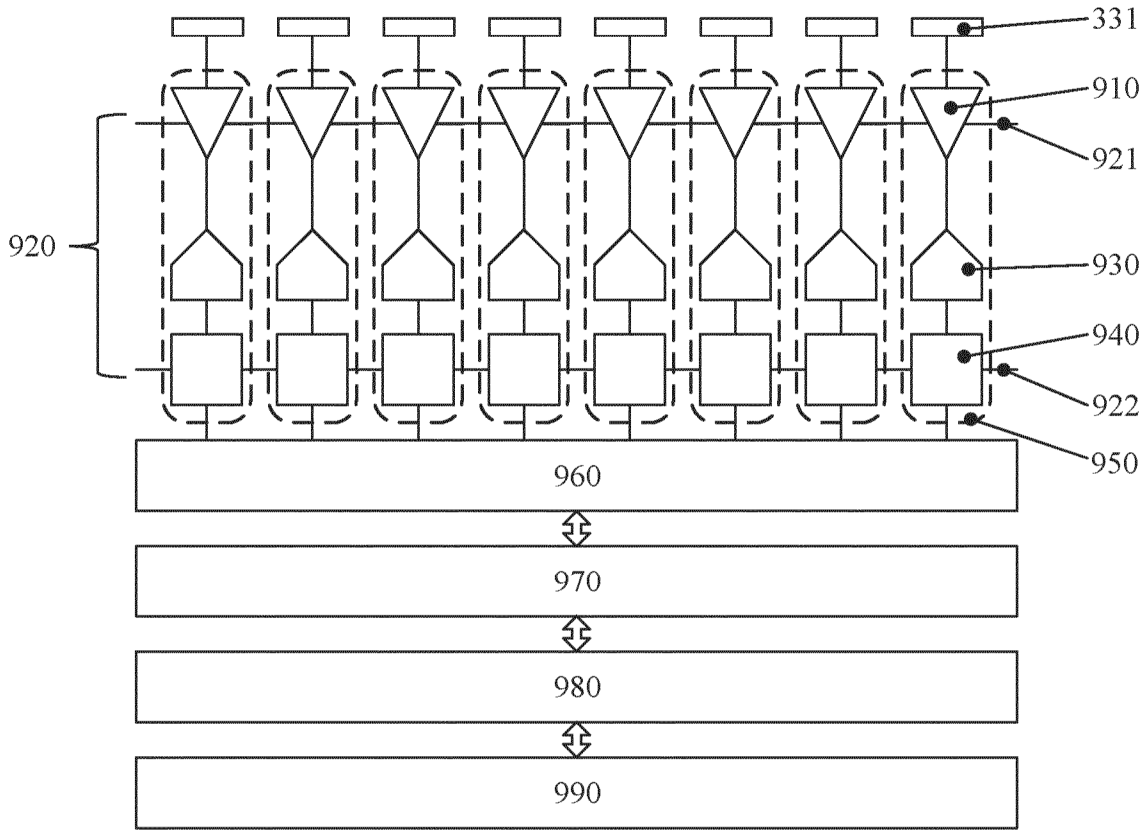


FIG. 9

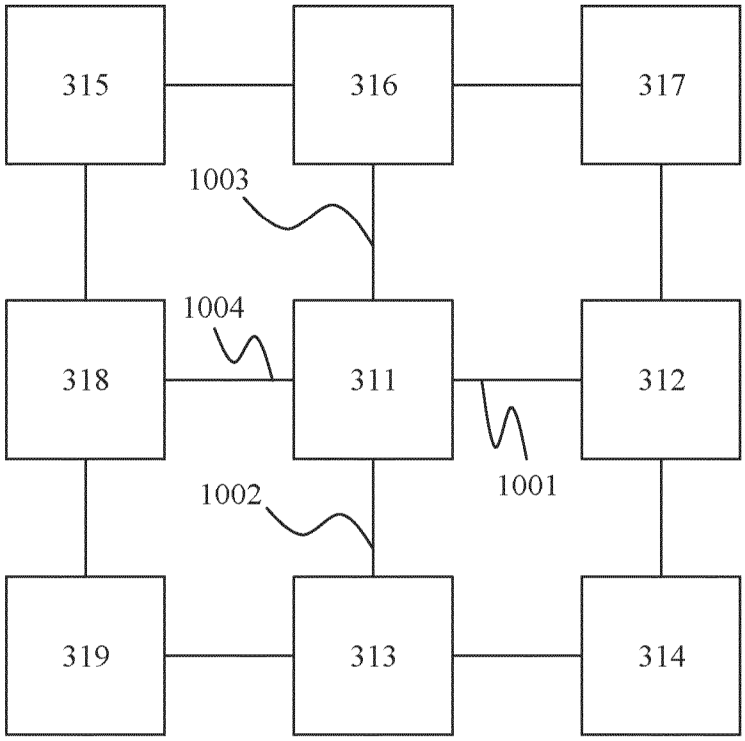


FIG. 10

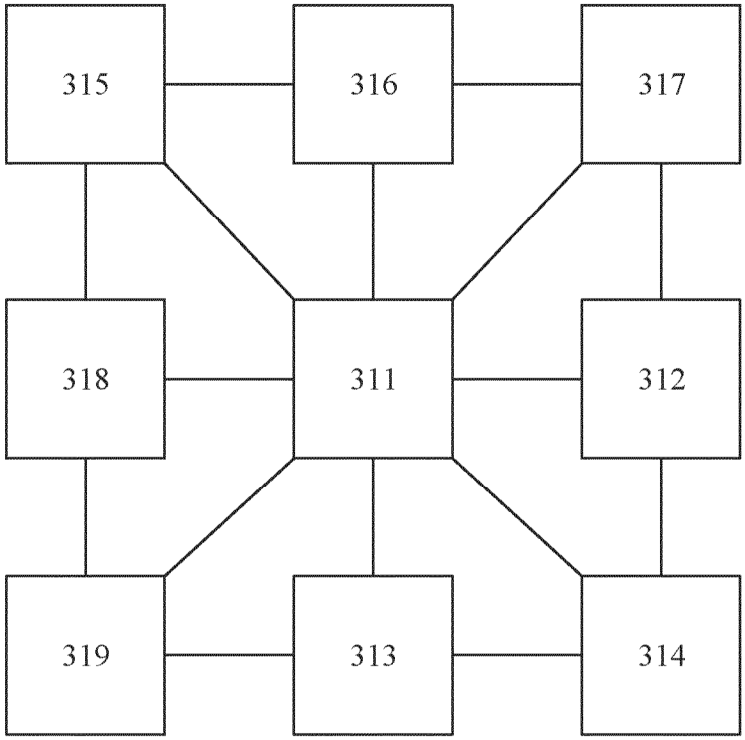


FIG. 11

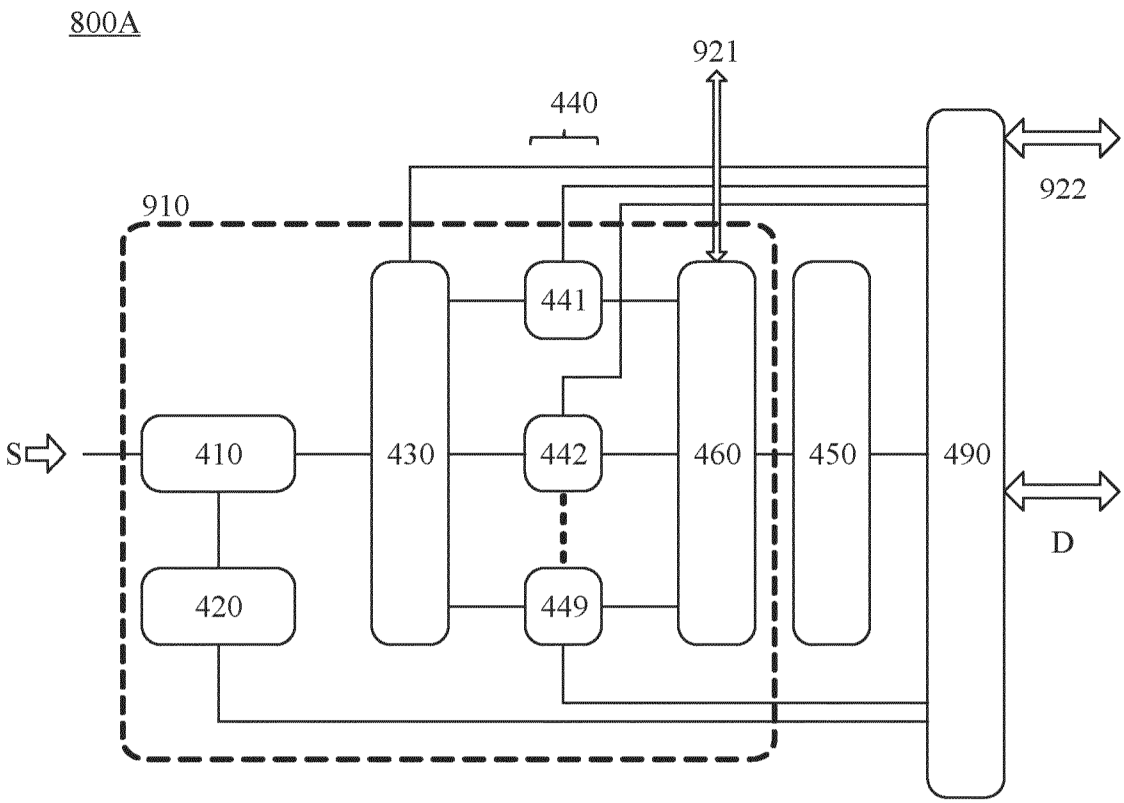


FIG. 12A

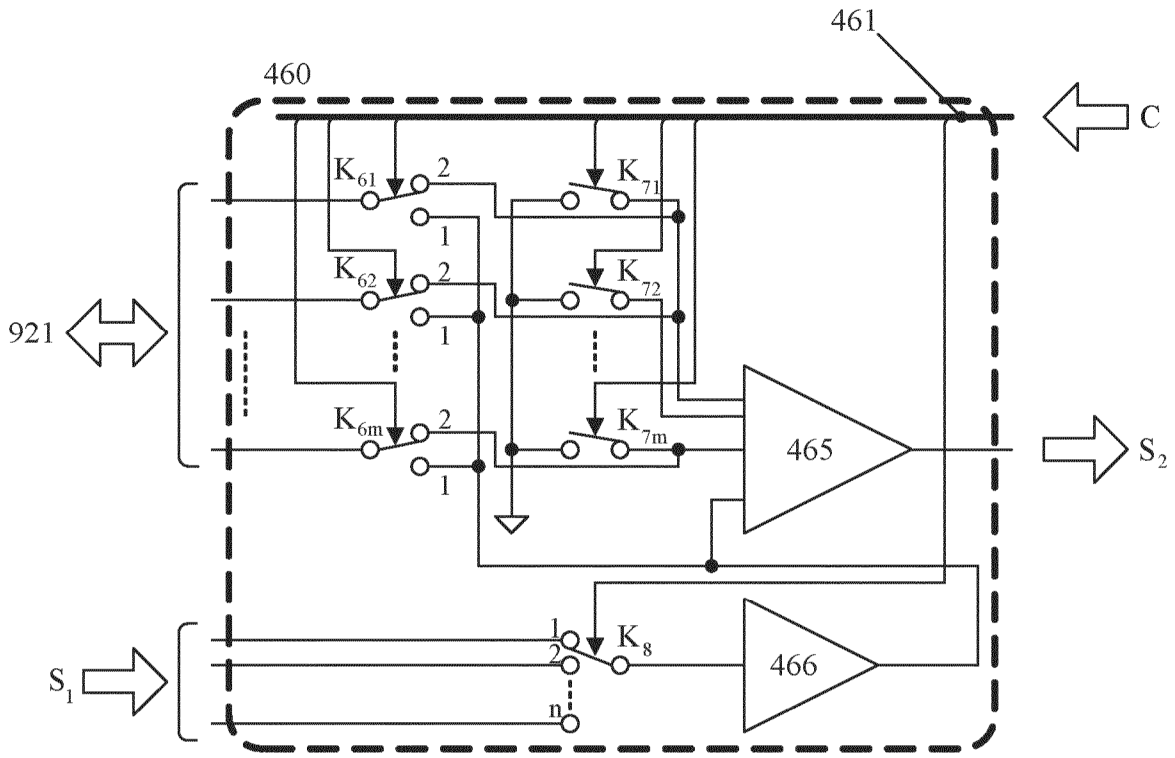


FIG. 12B

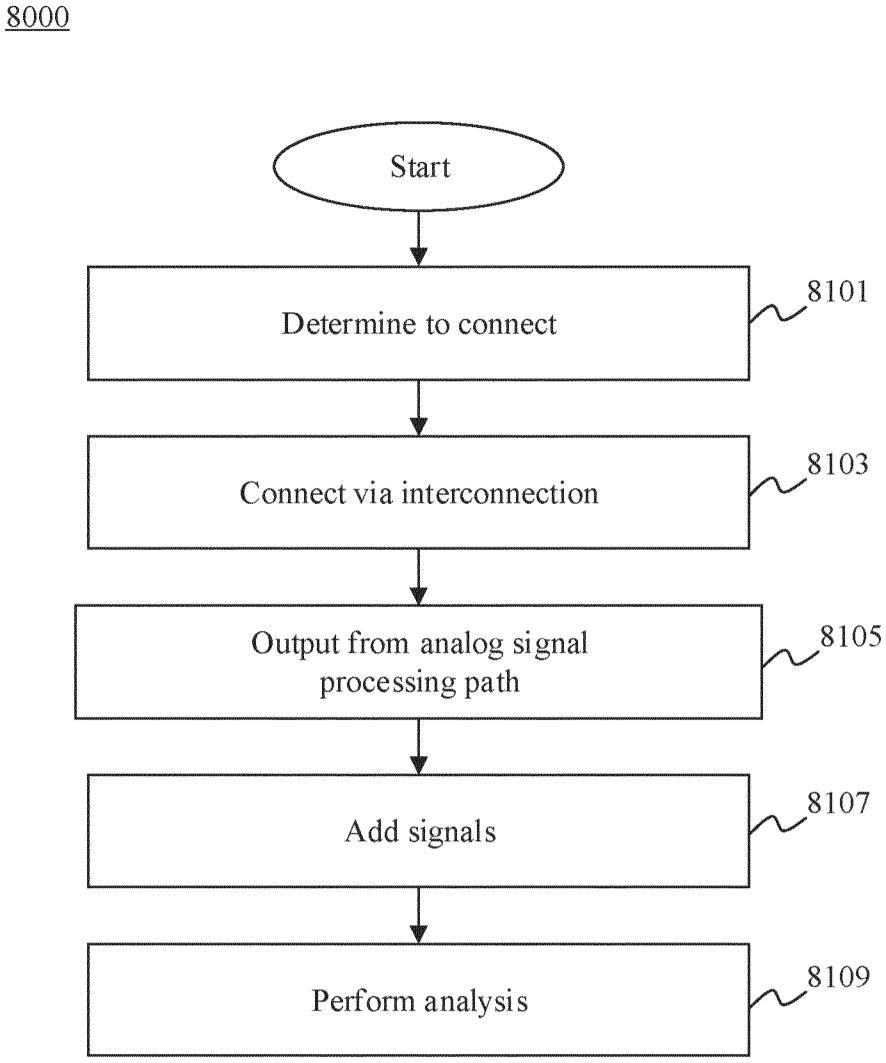

8000
Start
Determine to connect
8101
Connect via interconnection
8103
Output from analog signal processing path
8105
Add signals
8107
Perform analysis
8109

FIG. 13

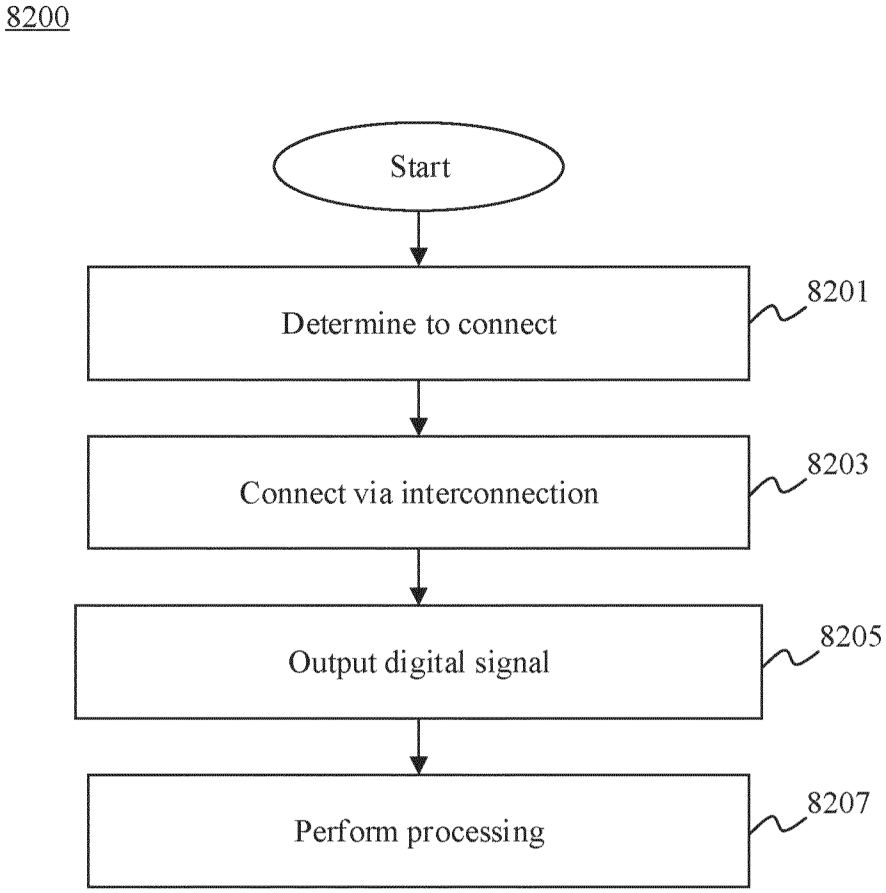

8200
Start
Determine to connect
8201
Connect via interconnection
8203
Output digital signal
8205
Perform processing
8207

FIG. 14

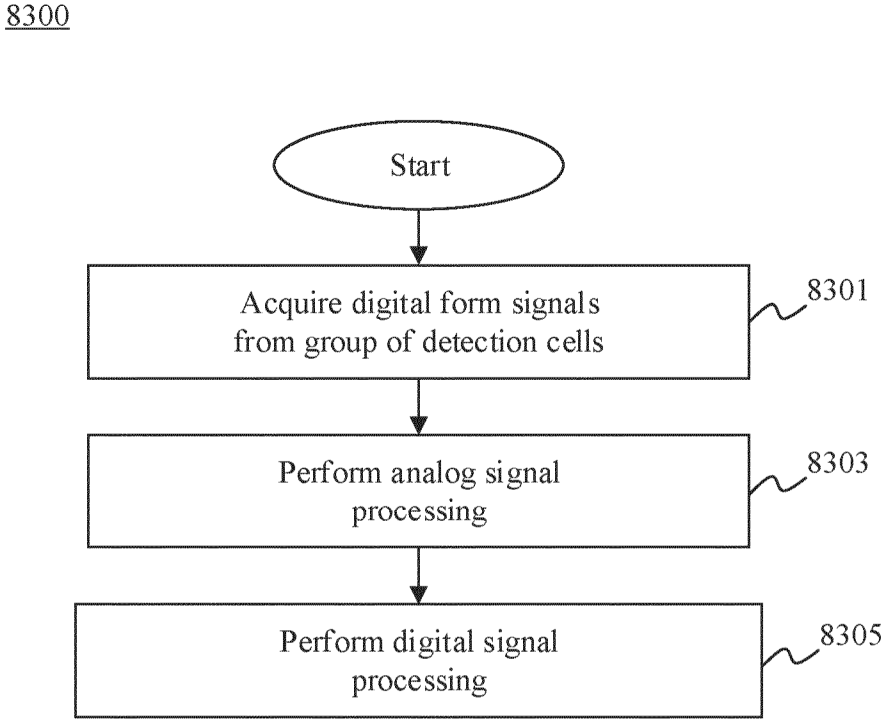

8300
Start
Acquire digital form signals from group of detection cells
8301
Perform analog signal processing
8303
Perform digital signal processing
8305

FIG. 15