

ABSTRACTDATA PROTECTION APPARATUS AND METHOD

5 A data protection apparatus has chip select logic
102, a protection circuit 101 and one or more memory
devices 11-13. The chip select logic is designed so that
when protected memory is addressed, more than one
selection signal is generated. In this way, a protected
10 memory area may encompass all, or a portion, of one or
more memory devices. The additional selection signal is
processed by the protection circuit which will interrupt
the processor if protected memory is addressed during a
write cycle in the absence of a request signal which the
15 processor is programmed to generate just prior to its
writing to a protected memory area.

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