

The invention is based on a circuit for raster correction in a television device according to the preamble of claim 1.

With this type of circuit, the value of the current fed to the correction coil is periodically altered by a small amount for the adjustment of the respective correction current required. The shift caused in the deflection raster by this alteration, i.e. the displacement of the raster in a vertical or horizontal direction, is so small that it cannot be perceived per se. However, if this small alteration of the deflection raster occurs periodically then it can be perceived as a shaking of the picture. This is particularly so if a grid pattern of horizontal and vertical white lines is presented on the screen.

It is the object of the invention to avoid the disturbing periodic motion within the deflection raster without impairing the entire function of the circuit with the oscillating motion about the desired value.

This object is achieved by the invention given in claim 1. Further advantageous developments of the invention are given in the sub-claims.

The invention is based on the following consideration. The described oscillating motion about the desired value is necessary in order to ensure that the actual value does not move away from the desired value slowly in one direction without this being registered by the circuit. However, it suffices if this oscillating motion occurs only periodically during a time when the picture is invisible e.g. during the vertical blanking interval or the horizontal blanking interval. This oscillating motion does not occur during the time when the picture is visible. The correction current is only acted upon during the visible deflection raster if the oscillating motion during the time when the picture is invisible represents too large a deviation. Consequently, the oscillating process is shifted and limited to the

picture region outside the visible picture area. There is advantageously obtained the combination of the necessary oscillating process with a stationary picture without disturbing periodic motion of the deflection raster.

An embodiment of the invention will be explained with reference to the drawing. There is shown

Fig. 1 a block circuit diagram of the circuit constructed according to the invention and

Fig. 2 curves for explaining the manner of operation.

In Fig. 2, the memory M1 contains correction values for the deflection raster. The memory M1 generates, via the switch 2 and the amplifiers 3, 4, a respective correction current i_K in the correction coil 5 for the convergence of picture elements which are defined on the screen by a grid pattern.

A memory cell in the memory M1 is addressed for each point of the grid pattern.

In addition to this dynamic correction of the convergence of successive picture elements another test process is to be carried out, e.g. in order to stabilize the static position of the picture - the so-called offset position. The memory M2 generates a test signal for this purpose which periodically arrives at the correction coil 5, via the switch 2 in the position shown by the broken line, instead of the correction signal from memory M1. Associated with the test signal is a test current i_T with a defined desired value which is to be generated respectively by the test signal. A deviation of the test current i_T from the desired value is to be compensated by the circuit. The desired value of the test current i_T based on the test signal can be e.g. zero. For this purpose, inserted into the low end of the correction coil 5 is the resistor 6, at which the voltage U_{s1} proportional to the test

current i_T appears. U_{s1} is fed to the comparator 7 which carries out a comparison with the desired value U_{soll} which serves as a reference.

The manner of operation is explained by means of Fig. 2. At time t_1 , the voltage U_{s1} proportional to the test current i_T has a value which lies beneath the desired value U_{soll} . Thereupon, the comparator 7 supplies the digital output voltage U_{s2} with the value "0". U_{s2} arrives at the microprocessor 10, which feeds the two memories M1 and M2. The memory M2 now receives the information, based on the supplied value of the voltage U_{s2} , that the test current i_T based on the test signal is too low. Thereupon, the test signal and the test current are raised by the step S. Within the next vertical blanking interval it is established that U_{s2} has not altered, i.e. has not yet used the correction introduced. Therefore, the test signal and the correction current thereby generated are increased by a further step S at time t_2 . U_{s1} is further increased by the step S at time t_3 during the next vertical blanking interval. With this increase, the desired value U_{soll} is reached whereupon the voltage U_{s2} assumes the value "1". This is a signal for the processor 10 and the memory M2 that the correction was successful, U_{s1} has reached its desired value and no further correction is necessary. In principle, the circuit could now remain in this condition with the adjusted test current and the thereupon supplied correction current i_K .

However, if a deviation in the opposite direction appears over a longer period of time and the voltage U_{s1} deviates in the opposite direction as shown by the broken curve K, the comparator 7 would no longer respond because its switching threshold was already reached at time t_3 . The entire circuit would no longer be able to register the deviation according to curve K. Therefore, after a certain time, the test signal is switched back by one step S at time t_4 . If the microprocessor 10 registers an alteration of U_{s2} from "1" to "0" upon this switching back, this is taken as an indication that the desired value U_{soll} has been maintained with the required

approximation, i.e. there exists merely a deviation from U_{sol} of one amplitude step S . This oscillating motion now further occurs periodically at times t_4 , t_5 , t_6 and t_7 .

The oscillating motion described only occurs during the vertical blanking interval or the horizontal blanking interval in which no visible picture is written. The oscillating motion does not occur during the time of the visible picture. During this time, the correction current is not subject to the oscillating motion and is constant as indicated by the curve i_K in Fig. 2. The correction current i_K is only corrected for the visible picture if the circuit registers a deviation of U_{s1} from the desired value U_{sol} greater than an amplitude step S . This correction happens, according to experience, relatively seldom because the entire circuit serves only to stabilize long-term fluctuations. According to experience, such a rare alteration of i_K and therewith, a change in the position of the deflection raster is not disturbing during this time. The circuit can also be constructed so that the alteration of the correction current i_K only occurs when the described deviation from the desired value U_{sol} amounts to several steps S , e.g., two, three or four steps.



CLAIMS

1. A circuit for raster correction in a television device with which, in a test process, a test signal is periodically supplied to the deflection circuit, the test current (i_T) flowing thereupon and a desired value (U_{oll}) are fed to a comparator (7) the digital output signal (U_{s2}) of which, via a processor (10), acts upon a memory (M2), which supplies the test signal, and alters the deflection current by one step (S) in each case until the deflection current oscillates about the desired value (U_{oll}) by one amplitude step (S), in which the processor (10) acts upon a memory (M1) which supplies the correction current (i_K) for the visible picture, **characterised in that** the test process with the oscillating motion only occurs during a time in which the picture is invisible and an alteration of the correction current (i_K) for the visible time of the picture only occurs when the test current (i_T) deviates by more than one step (S) from the desired value (U_{oll}).
2. A circuit according to claim 1, **characterised in that** the test process occurs in each case during the vertical blanking interval.
3. A circuit according to claim 1, **characterised in that** the test process occurs in each case during the horizontal blanking interval.
4. A circuit according to claim 1, **characterised in that** an input of an amplifier (3) supplying the correction deflector coil (5) is connected, in a periodically alternating way, via a change-over switch (2), with the output of a memory (M1) for the correction current (i_K) and with the output of a memory (M2) for the test current (i_T).
5. A circuit according to claim 1, **characterised in that** an alteration of the correction current (i_K) only occurs when the test current (i_T) deviates from the desired value (U_{oll}) by several steps (S).