ABSTRACT

A GLOBAL PLANARIZATION METHOD FOR INTER LEVEL DIELECTRIC LAYERS OF INTEGRATED CIRCUITS

The present invention provides a method of manufacturing of planarizing an insulating layer using a sized reversed interconnect mask and two polish stop layers. Spaced interconnections 14 are provided over the semiconductor substrate 10. An insulating layer 22 is formed over the interconnections 14 forming valleys 18 between the spaced interconnections 14. A first polish stop layer 26 is formed over the insulating layer 22. A dielectric layer 30 is formed over the first polish stop layer 26. A second polish stop layer 36 is formed over the dielectric layer 30. The top of the second polish stop layer 36 over the valley 23 is coplanar with the top of the first polish stop layer 26 over the interconnect 14. A reduced size, reverse interconnect mask 40 is formed over the second polish stop layer 36. The reduced size, reverse interconnect mask 40 covers portions of the valleys 23 between the spaced interconnections 14. The second polish stop layer 36 is etched using the reverse interconnect mask 40 as an etch mask leaving second polish stop blocks 36A over the narrow valleys 23. The dielectric layer 30 over the interconnections 14 is chemical-mechanical polished using the first polish stop layer 26 and second polish stop layer blocks 36A as a polish stop thereby providing the dielectric layer 30 with a planar top surface. The second polish blocks 36A eliminate the "dishing" problem associated with chemical-mechanical polishing processes.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)