

CYCLE INDEPENDENT DATA TO ECHO CLOCK TRACKING CIRCUIT

ABSTRACT

A comparator (40) and variable delay circuit are provided to maintain the tracking between data and echo clocks in a double data rate (DDR) RAM device. This is accomplished by providing a global data signal (dummy data signal) that tracks with the actual memory array data. This global data signal is compared to the timing of the RAM clock (CLOCK) (28) to determine a delay time between the two by which the pipeline clocks (CLKRISE/CLKFALL) must be delayed. As a result, the pipeline clocks are pushed out as needed so that they always transition after the array data arrives at the output latch. Therefore, as cycle time decreases, both echo clocks and data are pushed out identically and maintain their required tracking.

FIG 3