140 using an address of the interrupt table 150 (IRT@) provided by the copy of the DTE 146. The IRTE 152 provides a mapping of the interrupt target ID to a logical processor ID which is used by the bus attachment device 110 to address the target processor directly in case of a directed interrupt forwarding. The IRTE 152 may in addition provide a running indicator 154 indicating whether the target processor identified by the interrupt target ID is scheduled, i.e. running, at all and/or a blocking indicator 146 indicating whether the target processor is currently blocked from receiving interrupt signals. In case the target processor is not scheduled or temporarily block, a broadcast may be initiated in order enable a timely interrupt handling.

[0115] FIG. 13 is a flowchart of an exemplary method for providing an interrupt signal to a guest operating system using the computer system 100 of FIG. 100. The method of FIG. 11 continues after step 340 of FIG. 8 with step 342. In step 342, the bus attachment fetches a copy of an IRTE form the memory using the interrupt target ID received with the interrupt signal as well as an address indicator provided by the DTE indicating a memory of the IRT. In step 350, the bus attachment device updates the vectors specified in the DTE.

[0116] In step 360, the bus attachment device checks the direct signaling indicator provided with the interrupt signal. In case the direct signaling indicator indicates no direct signaling, the bus attachment device forwards the interrupt signal in step 370 by broadcasting using the zone identifier and the interrupt subclass identifier, in order to provide the interrupt signal to a processor used by the guest operating system. In case the direct signaling indicator indicates direct signaling, the bus attachment device further checks in step 362, whether a running indicator comprised by the copy of the IRTE indicates that the target processor identified by the interrupt target ID is running.

[0117] In case the target processor is not running, the bus attachment device in step 364 sends a broadcast interrupt as a fallback using, e.g., a logical partition ID and/or an interrupt subclass ID to identify processor suitable for handling the interrupt. In case no suitable processor matching the logical partition ID and/or the interrupt subclass ID is found, the hypervisor, i.e. a processor assigned for usage by the hypervisor, may receive the interrupt request instead of a processor assigned to the guest operation system. The hypervisor may decide on broadcasting the interrupt request again if one or more processors assigned to the guest operation system get scheduled. On an entry of a processor assigned to the operating

CLAIMS

1. A method for providing an interrupt signal to a guest operating system (204) executed using one or more processors of a plurality of processors (130) of a computer system (100) assigned for usage by the guest operating system (204), the computer system (100) further comprising one or more bus connected modules (120) being operationally connected with the plurality of processors (130) via a bus (102) and a bus attachment device (110), the computer system (100) further comprising a memory (140) operationally connected with the bus attachment device (110),

each processor of the plurality of processors (130) being assigned with a logical processor ID (222) used by the bus attachment device (110) to identify and address the respective processor (130),

each processor of the plurality of processors (130) assigned for usage by the guest operating system (204) further being assigned with an interrupt target ID used by the guest operating system (204) and one or more bus connected modules (120) to address the respective processor (130),

the memory (140) comprising a directed interrupt signal vector (162) per interrupt target ID assigned to the respective interrupt target ID,

the method comprising:

receiving by the bus attachment device (110) an interrupt signal from one of the bus connected modules (120) of the one or more bus connected modules (120), the interrupt signal including an interrupt target ID, the interrupt target ID identifying one of the processors (130) assigned for usage by the guest operating system (204) as a target processor (130) for handling the interrupt signal,

selecting by the bus attachment device (110) the directed interrupt signal vector (162) assigned to the interrupt target ID to which the received interrupt signal is addressed, wherein each directed interrupt signal vector (162) comprising a directed interrupt signal indicator per bus connected module (120) assigned to the respective bus connected module (120), each directed interrupt signal vector (162) indicating whether there is an interrupt signal issued by the respective bus connected module (120) and addressed to the respective interrupt target ID to be handled,

the directed interrupt signal vectors (162) each being implemented as a contiguous area in memory (140),

selecting by the bus attachment device (110) in the selected directed interrupt signal vector (162) the directed interrupt signal indicator assigned to the bus connected module (120) which issued the received interrupt signal,

updating by the bus attachment device (110) the selected directed interrupt signal indicator such that the respective directed interrupt signal indicator indicates that there is an interrupt signal issued by the respective bus connected module (120) and addressed to the respective interrupt target ID to be handled,

translating by the bus attachment device (110) the interrupt target ID assigned to the target processor (130) received with the interrupt signal to a logical processor ID (222) of the target processor (130), and

forwarding by the bus attachment device (110) the interrupt signal to the target processor (130), the forwarding using the logical processor ID (222) of the target processor (130) to address the target processor (130) as the target of the interrupt signal, wherein the interrupt signal comprises an indication of the selected directed interrupt signal vector (162).

2. The method of claim 1, the interrupt signal indicators assigned to the same bus connected module (120) each comprising the same offset within the directed interrupt signal vector (162) comprising the respective interrupt signal indicator.

3. The method of claim 1, the directed interrupt signal indicators each being implemented as a single bit.

4. The method of claim 1, the method further comprising retrieving by the bus attachment device (110) a copy of an interrupt table entry (152) assigned to the received interrupt target ID from an interrupt table (150) stored in the memory (140), the interrupt table entry (152) comprising a directed interrupt signal vector address indicator indicating a memory address of the directed interrupt signal vector (162) assigned to the interrupt target ID to which the received interrupt signal is addressed, the bus attachment device (110) using the memory address of the respective directed interrupt signal vector (162) for the selecting of the directed interrupt signal vector (162) assigned to the interrupt target ID to which the received interrupt signal is addressed.

5. The method of claim 4, the method further comprising retrieving by the bus attachment device (110) a copy of a device table entry (146) from a device table (144) stored in the memory (140), the device table entry (146) comprising an interrupt table address indicator indicating a memory address of the interrupt table (150), the bus attachment device (110) using the memory address of the interrupt table (150) for the retrieving of the copy of the interrupt table entry (152).

6. The method of claim 5, the device table entry (146) further comprising a directed interrupt signal offset indicator indicating an offset of the directed interrupt signal indicator assigned to the bus connected module (120) which issued the received interrupt signal.

7. The method of claim 1, the memory (140) further comprising a directed interrupt summary vector (160) with a directed interrupt summary indicator per interrupt target ID, each directed interrupt summary indicator being assigned to an interrupt target ID indicating whether there is an interrupt signal addressed to the respective interrupt target ID to be handled,

the method further comprising:

selecting by the bus attachment device (110) the directed interrupt summary indicator assigned to the interrupt target ID to which the received interrupt signal is addressed,

updating by the bus attachment device (110) the selected directed interrupt summary indicator such that the selected directed interrupt summary indicator indicating that there is an interrupt signal addressed to the respective interrupt target ID to be handled.

8. The method of claim 7, the directed interrupt summary vector (160) being implemented as a contiguous area in memory (140).

9. The method of claim 7, the directed interrupt summary indicators each being implemented as a single bit.

10. The method of claim 7, the interrupt table entry (152) further comprising a directed interrupt summary vector address indicator indicating a memory address of the directed interrupt summary vector (160), the bus attachment device (110) using the memory address of the

directed interrupt summary vector (160) for selecting the directed interrupt summary indicator assigned to the target processor ID to which the received interrupt signal is addressed.

11. The method of claim 7, the memory (140) further comprising an interrupt table entry (152) assigned to the received interrupt target ID, the interrupt table entry (152) comprising a directed interrupt summary offset indicator indicating an offset of the directed interrupt summary indicator assigned to the interrupt target ID within the directed interrupt summary vector (160).

12. The method of claim 1, the method further comprising retrieving by the bus attachment device (110) a copy of an interrupt table entry (152) assigned to the interrupt target ID from an interrupt table (150) stored in the memory (140), the copy of the interrupt table entry (152) comprising a current mapping of the interrupt target ID to a first logical processor ID (222), the bus attachment device (110) using the copy of the interrupt table entry (152) for the translating of the interrupt target ID of the target processor (130) received with the interrupt signal.

13. The method of claim 1, the method further comprising retrieving by the bus attachment device (110) a copy of a device table entry (146) from a device table (144) stored in the memory (140), the device table entry (146) comprising a direct signaling indicator indicating whether the target processor (130) is to be addressed directly, the direct signaling indicator indicating a direct forwarding of the interrupt signal being a requirement for executing the forwarding of the interrupt signal using the logical processor ID (222) of the target processor (130) to address the target processor (130) directly, else the forwarding being executed using broadcasting.

14. The method of claim 1, the method further comprising retrieving by the bus attachment device (110) a copy of an interrupt table entry (152) from an interrupt table stored (150) in the memory (140), the interrupt table entry (152) comprising a copy of a running indicator (154) indicating whether the target processor (130) identified by the interrupt target ID is scheduled for usage by the guest operating system (204), the target processor (130) being scheduled for usage by the guest operating system (204) being a further requirement for executing the forwarding of the interrupt signal using the logical processor ID (222) of the target processor (130) to address the target processor (130) directly, else the interrupt signal to the guest operating system for handling using broadcasting.

15. The method of claim 1, the method further comprising retrieving by the bus attachment device (110) a copy of an interrupt table entry (152) from an interrupt table (150) stored in the memory (140), the interrupt table entry (152) comprising an interrupt blocking indicator indicating whether the target processor (130) identified by the interrupt target ID is currently blocked from receiving interrupt signals, the target processor (130) being unblocked being a further requirement for executing the forwarding of the interrupt signal using the logical processor ID (222) of the target processor (130) to address the target processor (130) directly, else the interrupt signal to the guest operating system for handling using broadcasting.

16. The method of claim 1, the method further comprising retrieving by the bus attachment device (110) a device table entry (146) from a device table (144) stored in the memory (140), the device table entry (146) comprising a logical partition ID identifying a logical partition to which the guest operating system (204) is assigned, the forwarding of the interrupt signal by the bus attachment device (110) further comprising forwarding with the interrupt signal the logical partition ID.

17. The method of claim 1, the method further comprising retrieving by the bus attachment device (110) an interrupt subclass ID identifying an interrupt subclass to which the received interrupt signal is assigned, the forwarding of the interrupt signal by the bus attachment device (110) further comprising forwarding with the interrupt signal the interrupt subclass ID.

18. A computer system (100) for providing an interrupt signal to a guest operating system (204) executed using one or more processors of a plurality of processors (130) of the computer system (100) assigned for usage by the guest operating system (204), the computer system (100) further comprising one or more bus connected modules (120) being operationally connected with the plurality of processors (130) via a bus (102) and a bus attachment device (110) the computer system (100) further comprising a memory (140) operationally connected with the bus attachment device (110),

each processor of the plurality of processors (130) being assigned with a logical processor ID (222) used by the bus attachment device (110) to identify and address the respective processor (130),

each processor of the plurality of processors (130) assigned for usage by the guest operating system (204) further being assigned with an interrupt target ID used by the guest

operating system (204) and the one or more bus connected modules (120) to address the respective processor (130),

the memory (140) comprising a directed interrupt signal vector (162) per interrupt target ID assigned to the respective interrupt target ID,

the computer system (100) being configured to perform a method comprising:

receiving by the bus attachment device (110) an interrupt signal from one of the bus connected modules (120) of the one or more bus connected modules (120), the interrupt signal including an interrupt target ID, the interrupt target ID identifying one of the processors (130) assigned for usage by the guest operating system (204) as a target processor (130) for handling the interrupt signal,

selecting by the bus attachment device (110) the directed interrupt signal vector (162) assigned to the interrupt target ID to which the received interrupt signal is addressed, wherein each directed interrupt signal vector (162) comprising a directed interrupt signal indicator per bus connected module (120) assigned to the respective bus connected module (120), each directed interrupt signal vector (162) indicating whether there is an interrupt signal issued by the respective bus connected module (120) and addressed to the respective interrupt target ID to be handled; the directed interrupt signal vectors (162) each being implemented as a contiguous area in memory (140);

selecting by the bus attachment device (110) in the selected directed interrupt signal vector (162) the directed interrupt signal indicator assigned to the bus connected module (120) which issued the received interrupt signal,

updating the selected directed interrupt signal indicator such that the respective directed interrupt signal indicator indicates that an interrupt signal issued by the respective bus connected module (120) and addressed to the respective interrupt target ID is waiting to be handled,

translating the interrupt target ID assigned to the target processor (130) received with the interrupt signal to a logical processor ID (222) of the target processor (130),

forwarding the interrupt signal to the target processor (130), the forwarding using the logical processor ID (222) of the target processor (130) to address the target processor (130) as the target of the interrupt signal, wherein the interrupt signal comprises an indication of the selected directed interrupt signal vector (162).

19. A computer program product for providing an interrupt signal to a guest operating system (204) executed using one or more processors of a plurality of processors (130) of a computer

system (100) assigned for usage by the guest operating system (204), the computer system (100) further comprising one or more bus connected modules (120) being operationally connected with the plurality of processors (130) via a bus (102) and a bus attachment device (110) the computer system (100) further comprising a memory (140) operationally connected with the bus attachment device (110),

each processor of the plurality of processors (130) being assigned with a logical processor ID (222) used by the bus attachment device (110) to identify and address the respective processor (130),

each processor of the plurality of processors (130) assigned for usage by the guest operating system (204) further being assigned with an interrupt target ID used by the operating system and one or more bus connected modules (120) to address the respective processor (130), the memory (140) comprising a directed interrupt signal vector (162) per interrupt target ID assigned to the respective interrupt target ID,

the computer program product comprising a computer readable non-transitory medium readable by a processing circuit and storing instructions for execution by the processing circuit for performing a method comprising:

receiving by the bus attachment device (110) an interrupt signal from one of the bus connected modules (120) of the one or more bus connected modules (120), the interrupt signal including an interrupt target ID, the interrupt target ID identifying one of the processors (130) assigned for usage by the guest operating system (204) as a target processor (130) for handling the interrupt signal,

selecting by the bus attachment device (110) the directed interrupt signal vector (162) assigned to the interrupt target ID to which the received interrupt signal is addressed, wherein each directed interrupt signal vector (162) comprising a directed interrupt signal indicator per bus connected module (120) assigned to the respective bus connected module (120), each directed interrupt signal vector (162) indicating whether there is an interrupt signal issued by the respective bus connected module (120) and addressed to the respective interrupt target ID to be handled; the directed interrupt signal vectors (162) each being implemented as a contiguous area in memory (140);

selecting by the bus attachment device (110) in the selected directed interrupt signal vector (162) the directed interrupt signal indicator assigned to the bus connected module (120) which issued the received interrupt signal,

updating the selected directed interrupt signal indicator such that the respective directed interrupt signal indicator indicates that an interrupt signal issued by the

respective bus connected module (120) and addressed to the respective interrupt target ID is waiting to be handled,

translating the interrupt target ID assigned to the target processor (130) received with the interrupt signal to a logical processor ID (222) of the target processor (130),

forwarding the interrupt signal to the target processor (130), the forwarding using the logical processor ID (222) of the target processor (130) to address the target processor (130) as the target of the interrupt signal, wherein the interrupt signal comprises an indication of the selected directed interrupt signal vector (162).