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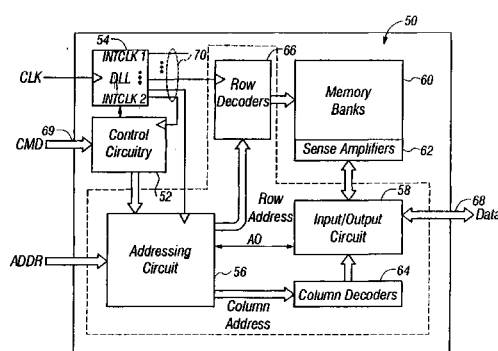
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(54) Title: MULTI-MODE SYNCHRONOUS MEMORY DEVICE AND METHOD OF OPERATING AND TESTING SAME



(57) Abstract: A synchronous semiconductor memory device is operable in a normal mode and an alternative mode. The semiconductor device has a command bus for receiving a plurality of synchronously captured input signals, and a plurality of asynchronous input terminals for receiving a plurality of asynchronous input signals. The device further has a clock input for receiving an external clock signal thereon, with the device being specified by the manufacturer to be operated in the normal mode using an external clock signal having a frequency no less than a predetermined minimum frequency. An internal delay locked loop (DLL) clocking circuit is coupled to the clock input terminal and is responsive in normal operating mode to be responsive to the external clock signal to generate at least one internal clock signal control circuitry in the device is responsive to a predetermined sequence of asynchronous signals applied to the device's asynchronous input terminals to place the device in an alternative mode of operation in which the internal clocking circuit is disabled, such that the device may be operated in the alternative mode using an external clock signal having a frequency less than the predetermined minimum frequency. The alternative mode of operation facilitates testing of the device at a speed less than the minimum frequency specified for the normal mode of operation.



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