

**SEMICONDUCTOR CHIP PACKAGE WITH ENHANCED
THERMAL CONDUCTIVITY**

This Sheet Has Been Replaced



ABSTRACT

5 A semiconductor chip package and method of making same wherein the
package comprises a ceramic substrate having two layers of thermally and
electrically conductive material (e.g., copper) on opposing surfaces thereof,
these layers thermally and electrically coupled by metal material located within
holes provided in the ceramic. A semiconductor chip is mounted on one of
these layers and the contact sites thereof electrically coupled to spaced
10 circuitry which, in a preferred embodiment, is formed simultaneously with
both thermally conductive layers. Coupling of the circuitry to an external
substrate (e.g., printed circuit board) is preferably accomplished using
metallic spring clips. These clips are preferably soldered in position. A
preferred metal for being positioned within the hole(s) is solder, one example
15 being 10:90 tin:lead solder. The package as produced herein may further
include two quantities of a protective encapsulant material located
substantially on the upper portions thereof to protect the chip and circuitry.
The preferred means for coupling the chip to the circuitry is to use a wire
bonding operation.