

30/04/03
200 3005335

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau



162162

(43) International Publication Date
10 May 2002 (10.05.2002)

PCT

(10) International Publication Number
WO 2002/037686 A3

(51) International Patent Classification⁷: **H03M 3/02**

(21) International Application Number:
PCT/US2001/046188

(22) International Filing Date: 31 October 2001 (31.10.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/703,647 1 November 2000 (01.11.2000) US

(71) Applicant: **QUALCOMM INCORPORATED** [US/US];
5775 Morhouse Drive, San Diego, CA 92121-1714 (US).

(72) Inventors: **BAZARJANI, Seyfollah**; 12906 Caminito
Beso, San Diego, CA 92130 (US). **WANG, Sean**;
3465 Lebon Drive #1717, San Diego, CA 92122 (US).
PELUSO, Vincenzo; 4259 Calle Mar De Ballenas, San
Diego, CA 92130 (US).

(74) Agents: **WADSWORTH, Philip, R.** et al.; Qualcomm In-
corporated, 5775 Morehouse Drive, San Diego, CA 92121-
1714 (US).

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU,
AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU,
CZ, DE, DK, DM, DZ, EC, EF, ES, FI, GB, GD, GE, GH,
GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC,
LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW,
MX, MZ, NO, NZ, PH, PL, PT, RO, RU, SD, SE, SG, SI,
SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA,
ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM,
KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian
patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European
patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE,
IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF,
CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD,
TG).

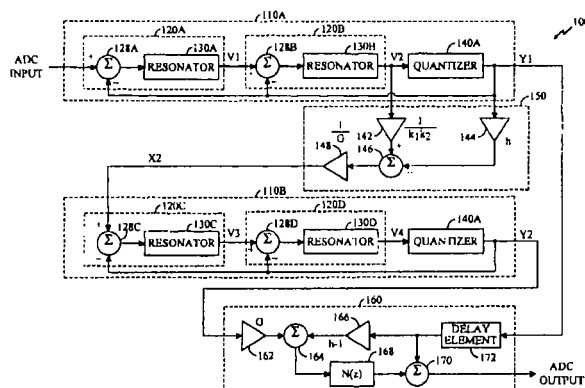
Published:

- with international search report
- before the expiration of the time limit for amending the
claims and to be republished in the event of receipt of
amendments

(88) Date of publication of the international search report:
19 February 2004

For two-letter codes and other abbreviations, refer to the "Guid-
ance Notes on Codes and Abbreviations" appearing at the begin-
ning of each regular issue of the PCT Gazette.

(54) Title: METHOD AND APPARATUS FOR CONTROLLING STAGES OF A MULTI-STAGE CIRCUIT



(57) Abstract: A control mechanism that can be used to control a $\Sigma\Delta$ to provide the required level of performance while reducing power consumption. The $\Sigma\Delta$ ADC is designed with multiple stage (i.e., loops or sections), and provides improved performance (e.g., higher dynamic range) as more stages are enabled. The control mechanism selectively enables a sufficient number of stages to provide the required performance and disables remaining stages to conserve power. The control mechanism achieves this by measuring one or more characteristics (e.g., signal level) of the ADC input signal through a $\Sigma\Delta$ ADC that is similar to the $\Sigma\Delta$ ADC on the signal path, comparing the measured characteristic(s) to particular threshold level(s), and controlling the stages such that the desired objectives are achieved. In one implementation, the control circuit includes one or more detector stages, a conditioning circuit, and a signal processor. The detector stage(s) receive the input signal and provide a detected signal. The conditioning circuit receives the detected signal and provides conditioned samples. The signal processor receives the conditioned samples and provides a control signal that selectively disables zero or more $\Sigma\Delta$ stages in the $\Sigma\Delta$ ADC.

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