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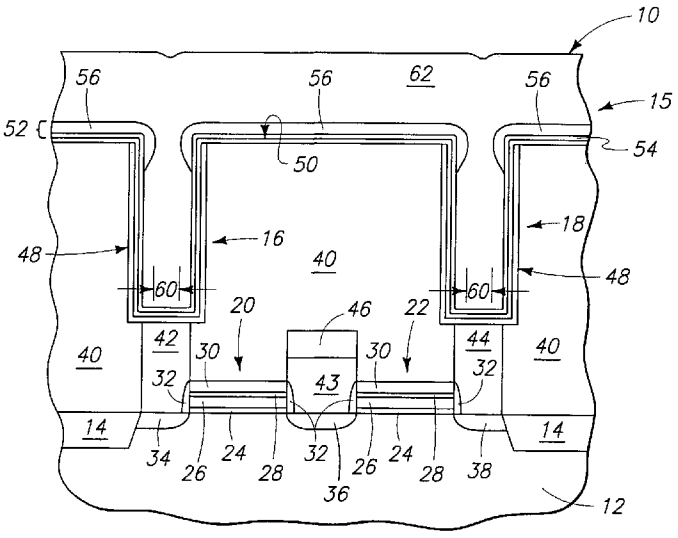
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(54) Title: TOP ELECTRODE FOR A DRAM CAPACITOR



(57) Abstract: The invention includes memory circuitry. In one implementation, memory circuitry includes a memory array (15) comprising a plurality of memory cell capacitors (16,18). Individual of the capacitors include a storage node electrode (48), a capacitor dielectric region (50), and a cell electrode (52). The cell electrode is commonly shared among at least some of the plurality of memory cell capacitors within the memory array. The cell electrode within the memory array includes a conductor metal layer (56) including at least one of elemental tungsten, a tungsten alloy, tungsten silicide and tungsten nitride. Polysilicon (62) is received over the conductor metal layer. The conductor metal layer and the polysilicon are received over the storage node electrodes of said at least some of the plurality of memory cell capacitors. Other aspects and implementations are contemplated.

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