

PLASMA CHAMBER SYSTEM AND METHOD OF ASHING PHOTORESIST
PATTERN FORMED ON SUBSTRATE HAVING LOW-K DIELECTRIC LAYER
USING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

This U.S. non-provisional patent application claims priority under 35 U.S.C. § 119 of Korean Patent Application 2004-97461 filed on November 25, 2004, the entire contents of which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor manufacturing apparatus and method of manufacturing a semiconductor device using the same, and more particularly to a plasma chamber system and method of ashing a photoresist pattern formed on a substrate having a low-K dielectric layer using the same.

In order to cope with requirements of making highly integrated semiconductor elements minute and highly integrated and of increasing the driving speed of the highly integrated semiconductor elements, researches on forming interlevel (or intermetal) insulation layers of low-K dielectric materials have been widely performed. Since the dielectric ratio of SiO₂ that is widely used as an interlevel insulation layer is 3.9 to 4.2, which is too high, it is not appropriate to use SiO₂ as the interlevel insulation layer for increasing the driving speed of the semiconductor elements. In particular, according to the road map of the International Technology Roadmap for Semiconductor (ITRS), it is expected that a material used as wiring lines be changed from current Al to Cu with low electric resistance in a semiconductor element whose critical dimension is 0.13μm and whose driving speed

is no less than 2,100MHz. In such a case, the interlevel material of a metal wiring line must be formed of a material having a dielectric constant of no more than 3.0.

[TABLE 1]

ITRS Road Map

Year of First Product Shipment	2000	2001	2002	2003	2004	2005
DRAM Half Pitch (2000 Litho ITRS)	150	130	115	100	90	80
MPU Half Pitch (2000 Litho ITRS)	180	150	130	115	100	90
Number of metal levels with ground planes	6-7	9-10	10	10-11	10-11	11
Interlevel metal bulk dielectric constant	2.9	2.7	2.7	2.0	2.0	1.3
Interlevel metal effective dielectric constant	3.5-4.0	2.9-3.5	2.9-3.5	2.2-2.9	2.2-2.9	1.6-2.2

In particular, as suggested in TABLE 1, low-K dielectric materials whose bulk dielectric constant is no more than 2.0 are expected to be applied to highly integrated semiconductor elements after 2004. This is because, when the low-K dielectric materials are not used as interlevel insulation layers in the development of semiconductor elements whose critical dimension is no more than 0.13 μ m, parasitic capacitance that causes RC delay, increase in power consumption, and noise due to mutual interference rapidly increases between wiring lines. Since the increase in the parasitic capacitance becomes an obstacle to increasing the driving speed of semiconductor elements, to reducing the power consumption of the semiconductor elements, and to making the semiconductor elements highly integrated, as described above, researches on using the low-K dielectric materials as the interlevel insulation layers are performed.

However, when the low-K dielectric materials are used as the interlevel insulation layers, it is difficult to perform the ashing process for removing the photoresist pattern. This is because the conventional ashing process is performed using an O₂ gas at high temperature such that the low-K dielectric characteristic of the interlevel insulation layer deteriorates and that mechanical firmness is reduced.

To be specific, in order to reduce the dielectric ratio of the interlevel insulation layer, in a process of forming the interlevel insulation layer, a process gas such as H₂ and CH₃ is added or a pore is formed in the interlevel insulation layer. At this time, the conventional ashing process includes a process of directly heating a chuck on which semiconductor substrates are loaded or heating a process chamber at the temperature of no less than 250°C by additional heating means such as a halogen lamp and then, supplying an O₂ gas and an additive gas to the heated process chamber. In such a high temperature process, the O₂ gas is decomposed into O₂ radicals used for removing photoresist.

However, the O₂ radicals that are in isotropic motions permeate into the interlevel insulation layer through the exposed side walls (for example, the inner wall of a hole) of the interlevel insulation layer to be combined with H₂ or CH₃ or to destroy the pore such that the low-K dielectric characteristic or the mechanical firmness deteriorates. When a photograph (refer to FIG. 1A) taken before performing the ashing process is compared with a photograph (refer to FIG. 1B) taken after performing the ashing process, it is noted that the side walls of the interlevel insulation layer with the low-K dielectric characteristic are significantly damaged after performing the ashing process. Since the activity of the O₂ radicals increases at high temperature, it is difficult to apply the ashing process in which the O₂ radicals

are used at the high temperature to the interlevel insulation layer with the low-K dielectric characteristic.

In order to prevent the low-K dielectric characteristic of the interlevel insulation layer from deteriorating due to the O_2 radicals, another ashing process of using H_2 and He at high temperature is suggested. Since the reducing operation of H_2 is used for the ashing process, the physical characteristics of the low-K dielectric layer are not changed due to the ashing process. However, according to the ashing process, since the ashing rate is low, productivity is low and the ashing process must be performed at high temperature.

On the other hand, it is difficult to perform the ashing process in which the O_2 radicals are used since the ashing process must be performed at high temperature in order to activate the O_2 radicals. Therefore, in order to solve the problem, it is requested to develop a plasma chamber system that can activate the O_2 radicals at low temperature.

However, a commonly used capacity coupling plasma chamber system is effective to increasing etching ratio by increasing the concentration of the plasma formed in the chamber, however, cannot control the uniformity of plasma in accordance with position. As a result, according as substrates are recently made larger, plasma chamber systems capable of compensating for increase in the concentration of plasma and the non-uniformity in the concentration of plasma in accordance with position are required.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a plasma chamber system capable of compensating for increase in the concentration of plasma and the non-uniformity in the concentration of plasma in accordance with position.

It is another object of the present invention to provide a plasma chamber system capable of removing photoresist formed on a low-K dielectric layer without deteriorating the characteristic of the low-K dielectric layer.

It is another object of the present invention to provide an ashing method capable of removing photoresist without damaging the low-K dielectric layer.

It is another object of the present invention to provide an ashing method capable of removing photoresist at low temperature.

In order to achieve the first and second objects, there is provided a plasma chamber system comprising independently controlled Helmholtz coils on and under a process chamber. The plasma chamber system comprises a process chamber, a wafer chuck arranged in the process chamber, a bottom radio-frequency power source electrically connected to the wafer chuck, a top electrode arranged on the wafer chuck, top Helmholtz coils arranged on the process chamber, and bottom Helmholtz coils arranged under the process chamber.

According to embodiments of the present invention, the plasma chamber system further comprises a top power source for supplying first current to the top Helmholtz coils and a bottom power source for supplying second current to the bottom Helmholtz coils. At this time, the first current is preferably direct current of -10 through 10 A and the second current is preferably direct current of -10 through 10 A.

Also, a controller is connected to the top power source and the bottom power source to control the magnitude of the first current and the second current

such that the concentration and uniformity of the plasma generated in the process chamber are corrected.

In order to achieve the third and fourth objects, there is provided a method of ashing a photoresist pattern capable of activating O_2 radicals at low temperature. The method comprises the steps of forming a low-K dielectric layer on a semiconductor substrate, forming a photoresist pattern on the semiconductor substrate including the low-K dielectric layer, loading the semiconductor substrate including the photoresist pattern in an ashing chamber including top Helmholtz coils and bottom Helmholtz coils and a top electrode and a bottom electrode, and removing the photoresist pattern while supplying an ashing gas including O_2 to the inside of the ashing chamber. At this time, in the step of removing the photoresist pattern, first direct current and second direct current are applied to the top Helmholtz coils and the bottom Helmholtz coils, respectively, while maintaining the inner temperature of the ashing chamber in 0 through $80^{\circ}C$.

According to embodiments of the present invention, the ashing gas comprises at least one gas among a N_2 gas, an inactive gas, a reduced gas, and a CF based gas and an O_2 gas. For example, the ashing gas comprises at least one gas among a N_2 gas, a He gas, an Ar gas, a H_2 gas, a H_2He gas, a H_2N_2 gas, CF_4 , and CHF_3 and an O_2 gas. At this time, the ashing gas is preferably supplied to the ashing chamber with a flow rate of 30 through 3,000sccm.

Also, the first direct current and the second direct current may be independently controlled in order to control the concentration of the plasma formed in the ashing chamber in accordance with position. According to the present invention, the first current and the second current may be controlled in the range of -10 through 10 A, respectively.

In the step of removing the photoresist, power of about 100 to 2,500 W is preferably applied to the bottom electrode and the inner pressure of the ashing chamber is preferably maintained as 10 to 600 mT.

The low-K dielectric layer can be formed of one material selected among methylsilsesquioxane (MSQ), hydrogen silsesquioxane (HSQ), SiOF, SiOC, a-uorocarbon, SiLK, polyimides, spin-on-glasses, fluorinated polyimides, diamond-like carbon (DLC), Cyclotenes, Parylene N, Poly (arylene ethers), Poly (arylenes), Poly (norbornens), Polyimide-SSQ hybrids, Alkyl-silanes/N₂O, Teflon-AF, Teflon microemulsion, Polyimide nanofoams, silica aerogels, silica xerogels, and Mesoporous silica.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate example embodiments of the present invention and, together with the description, serve to explain principles of the present invention. In the drawings:

FIGs. 1A and 1B are scanning electron microscope photographs illustrating the sections of an interlevel insulation layer before and after a conventional ashing process in order to describe the problems of the conventional ashing method;

FIG. 2 schematically illustrates a plasma chamber system according to the present invention;

FIGs. 3 and 4 are graphs illustrating the effects of the plasma chamber system according to the present invention;

FIG. 5 is a flowchart illustrating a method of ashing a photoresist pattern formed on a substrate having a low-K dielectric layer according to the present invention;

FIG. 6 is a sectional view illustrating the ashing process according to the present invention and the characteristics thereof; and

FIGs. 7A and 7B are scanning electron microscope photographs illustrating the sections of an interlevel insulation layer before and after the ashing process, showing the effects of the ashing process according to the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will be described below in more detail with reference to the accompanying drawings. The present invention may, however, be embodied in different forms and should not be constructed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. It will also be understood that when a layer is referred to as being "on" another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present.

FIG. 2 schematically illustrates a plasma chamber system according to the present invention.

Referring to FIG. 2, a plasma chamber system 100 according to the present invention includes a process chamber 130, a supply pipe 170 for supplying process gases to the process chamber 130, and a valve device 140 for controlling

process pressure in the process chamber 130. A vacuum pump 150 for exhausting the process gases and reactants at uniform speed is connected to the valve device 140. While the process is performed, the inner pressure of the process chamber 130 is preferably maintained in 10 through 600 mT and the temperature of the process chamber 130 is preferably maintained in 0 through 80°C. Therefore, the vacuum pump 150 is preferably a turbo molecular pump (TMP).

Furthermore, a chuck 180 on which a substrate is provided is arranged in the process chamber 130 and a refrigerant pipe 220 to which refrigerant is supplied is connected to the chuck 180. The substrate 200 is controlled to have predetermined temperature while a process is performed by the refrigerant. The chuck 180 serves as a bottom electrode for forming plasma. Therefore, the chuck 180 is electrically connected to a bottom RF generator 120 arranged outside the process chamber 130. The bottom electrode 180 receives power from the bottom RF generator 120 to dissociate the process gas supplied to the process chamber 130 into ions, electrons, and neutral radicals. According to embodiments of the present invention, the bottom RF generator 120 can supply power whose frequency is about 13.56MHz with 100 through 2,500 W.

A baffle 160, a top electrode 210, and a channel 230 for controlling the flow of the process gases supplied through the supply pipe 170 are arranged in the process chamber 130. The baffle 160 and the top electrode 210 are arranged in the process chamber 130 such that the process gasses are uniformly diffused. The channel 230 is arranged in the process chamber 130 such that the process gasses and the reactants are uniformly exhausted to the outside of the process chamber 130. At this time, the top electrode 210 may be electrically connected to a top RF generator 250 arranged outside the process chamber 130.

A gate door 240 for taking in or out the substrate 200 is arranged on the side wall of the process chamber 130. The gate door 240 is closed while a process is performed such that the pressure inside the process chamber 130 is maintained highly vacuumous.

Top Helmholtz coils 11 and bottom Helmholtz coils 112 that can be independently controlled are arranged on and under the process chamber 130. A top power source 113 and a bottom power source 114 for supplying first current and second current are arranged in the top and bottom Helmholtz coils 111 and 112. The top power source 113 and the bottom power source 114 are controlled by a predetermined controller 250. The controller 250 controls the magnitudes of the first current and the second current in order to correct the concentration and uniformity of the plasma generated in the process chamber 130. According to the embodiments of the present invention, each of the first current and the second current is preferably DC current of -10 through 10 A in order to prevent magnetic field from being shielded by the process chamber 130, however, may vary if necessary.

According to an embodiment, plasma 99 formed in the process chamber 130 may be concentrated on the top of the substrate 200 by controlling the magnetic field formed by the top and bottom Helmholtz coils 111 and 112. In such a case, the concentration of the plasma 99 increases such that it is possible to increase the productivity of a process.

FIGs. 3 and 4 are graphs illustrating the effects of the plasma chamber system according to the present invention. FIG. 3 is a simulation result illustrating the magnitude of the magnetic field formed in the process chamber 130 when current applied to the top Helmholtz coils 111 changes to 0, 4, and -4 A while applying current of 4 A to the bottom Helmholtz coils 112 illustrated in FIG. 2. It is noted

from FIG. 3 that the magnitude of the magnetic field generated in the process chamber 130 can be controlled by controlling the magnitude of the current applied to the top Helmholtz coils 111 and the bottom Helmholtz coils 112. The configuration of the top and bottom Helmholtz coils 111 and 112 may vary in order to spatially minutely control the magnitude of the magnetic field.

FIG. 4 is a graph illustrating the ashing rate and the uniformity measured by the ashing device that adopts the plasma chamber system illustrated in FIG. 2.

Referring to FIG. 4, the graph of the reference numeral 1 is obtained when no current is applied to the top Helmholtz coils 111 and the bottom Helmholtz coils 112, the graph of the reference numeral 2 is obtained when current of 4 A is applied to the top Helmholtz coils 111 and the bottom Helmholtz coils 112, respectively, and the graph of the reference numeral 3 is obtained when current of 4 A and current of -4 A are applied to the top Helmholtz coils 111 and the bottom Helmholtz coils 112, respectively.

It is noted from the experiments that, when the same current is applied to the two kinds of coils 111 and 112 (refer to the graph 2), similar uniformity is maintained to the case in which no current is applied and the ashing rate increases. This is because, as illustrated in FIG. 3, an axial uniform magnetic field formed by overlapping magnetic fields affects the acceleration of electrons in the plasma 99 such that the concentration of the plasma increases.

On the other hand, when currents in different directions are applied to the two kinds of coils 111 and 112 (refer to the graph 3), the ashing rate increases at the edge of the substrate than in the center of the substrate. This is because, as illustrated in FIG. 3, a non-uniform magnetic field is formed in accordance with the

distance of the radius of a wafer such that the effect of increasing the concentration of the plasma due to the confinement of secondary electrons on the substrate is larger at the edge of the substrate. When the ashing rate is slower at the edge of the substrate than in the center of the substrate, the ashing process to which such an offset condition is applied can guarantee the non-uniformity thereof.

FIG. 5 is a flowchart illustrating an ashing method according to the present invention of removing the photoresist pattern formed on the semiconductor substrate. FIG. 6 is a sectional view illustrating the ashing process of removing the photoresist pattern formed on an interlevel insulation layer with a low-K dielectric characteristic.

Referring to FIGs. 5 and 6, an interlevel insulation layer with a low-K dielectric characteristic 320 is formed on a semiconductor substrate 200 S10. The interlevel insulation layer 320 can be formed of at least one material selected from methylsilsesquioxane (MSQ), hydrogen silsesquioxane (HSQ), SiOF, SiOC, fluorocarbon, SiLK, polyimides, spin-on-glasses, fluorinated polyimides, diamond-like carbon (DLC), Cyclotenes, Parylene N, Poly(arylene ethers), Poly(arylenes), Poly(norbornenes), Polyimide-SSQ hybrids, Alkyl-silanes/N₂O, Teflon-AF, Teflon microemulsion, Polyimide nanofoams, silica aerogels, silica xerogels, and Mesoporous silica. In the step 10 of forming the interlevel insulation layer 320, as illustrated in the conventional art, process gasses such as H₂ and CH₃ may be added. Pores for reducing dielectric ratio may be formed in the interlevel insulation layer 320.

A photoresist pattern 330 used as an etching mask is formed on the resultant material in which the interlevel insulation layer 320 is formed S20. The photoresist pattern 330 may be used as an ion implantation mask. The step of

forming the photoresist pattern 330 includes the step of forming an aperture that exposes the interlevel insulation layer 320 in a predetermined region through exposing and developing processes after forming a photoresist layer using a spin-coating method. Before forming the photoresist layer, an auxiliary layer 325 such as reflection preventing layer, an etching stop layer, and a protective layer may be further formed on the interlevel insulation layer 320.

Subsequently, an aperture 327 that exposes the under layer thereof is formed in a predetermined region by patterning the interlevel insulation layer 320 S30. Therefore, the side walls of the interlevel insulation layer 320 are exposed by the aperture 327. The patterning process is preferably performed by anisotropic etching using the photoresist pattern 320 as an etching mask.

After performing the patterning process, the photoresist pattern 330 used as the etching mask is removed S40. At this time, since the side walls of the interlevel insulation layer 320 are exposed, when the conventional ashing process performed using O_2 or H_2 at high temperature is applied, as illustrated in the conventional art, the dielectric characteristic may deteriorate or the interlevel insulation layer may be mechanically damaged. Such a problem may be overcome by performing the ashing process using the plasma chamber system that includes the top and bottom Helmholtz coils 111 and 112 as described above.

To be specific, while the process chamber 130 is maintained at the temperature of about 0 to 80°C, an ashing gas is supplied to the process chamber 130 through the supply pipe 170 with a flow rate of 30 through 3,000sccm. At this time, the inner pressure of the process chamber 130 is preferably maintained as 10 to 600mT. In addition, power of 100 through 2,500 W is applied to the chuck 180. Therefore, ions 350 generated by the ashing gas move toward the top surface of the

substrate 200 as illustrated in FIG. 6. The O₂ radicals 340 are activated by colliding with the ions 350. The activated O₂ radicals 340 remove the photoresist.

On the other hand, the concentration of the plasma formed on the substrate 200 increases and is controlled by the magnetic field controlled by the top and bottom Helmholtz coils 111 and 112. As a result, the concentration of the ions 350 that activate the O₂ radicals 340 increases. Therefore, the O₂ radicals 340 can effectively remove the photoresist pattern 330 under a process condition in which the temperature is not high unlike in the conventional art.

As a result, the profile of the interlevel insulation layer on which the ashing process according to the present invention is performed (refer to FIG. 7B) is the same as the profile of the interlevel insulation layer on which the ashing process is not performed (refer to FIG. 7A). That is, according to the ashing process of the present invention, it is possible to remove the photoresist pattern without damaging the interlevel insulation layer with the low-K dielectric characteristic.

According to the present invention, the top and bottom Helmholtz coils that can be independently controlled are arranged on and under the plasma process chamber. Therefore, the concentration of the plasma generated in the process chamber can be controlled in accordance with position.

Also, it is possible to remove the photoresist without damaging the low-K dielectric layer under the process condition in which the temperature is not high by performing the ashing process using the plasma process chamber.

WHAT IS CLAIMED IS:

1. A plasma chamber system comprising:
 - a process chamber;
 - a wafer chuck arranged in the process chamber;
 - a bottom radio-frequency power source electrically connected to the wafer chuck;
 - a top electrode arranged on the wafer chuck;
 - top Helmholtz coils arranged on the process chamber; and
 - bottom Helmholtz coils arranged under the process chamber.
2. The plasma chamber system as set forth in claim 1, further comprising:
 - a top power source supplying first current to the top Helmholtz coils; and
 - a bottom power source supplying second current to the bottom Helmholtz coils,
 - wherein the first current is direct current of -10 through 10 A, and
 - wherein the second current is direct current of -10 through 10 A.
3. The plasma chamber system as set forth in claim 2, further comprising a controller connected to the top power source and the bottom power source to control the magnitude of the first current and the second current such that the concentration and uniformity of the plasma generated in the process chamber are corrected.
4. A method of ashing a photoresist pattern, comprising the steps of:
 - forming a low-K dielectric layer on a semiconductor substrate;

forming a photoresist pattern on the semiconductor substrate including the low-K dielectric layer;

loading the semiconductor substrate including the photoresist pattern in an ashing chamber including top Helmholtz coils and bottom Helmholtz coils arranged on and under the ashing chamber and a top electrode and a bottom electrode arranged in the ashing chamber; and

removing the photoresist pattern while supplying an ashing gas including O₂ to the inside of the ashing chamber,

wherein, in the step of removing the photoresist pattern, first direct current and second direct current are applied to the top Helmholtz coils and the bottom Helmholtz coils, respectively, while maintaining the inner temperature of the ashing chamber in 0 through 80°C.

5. The method of ashing a photoresist pattern as set forth in claim 4, wherein the ashing gas comprises at least one gas selected among the group consisting of a N₂ gas, an inactive gas, a reduced gas, and a CF based gas and an O₂ gas.

6. The method of ashing a photoresist pattern as set forth in claim 4, wherein the ashing gas comprises at least one gas selected among the group consisting of a N₂ gas, a He gas, an Ar gas, a H₂ gas, a H₂He gas, a H₂N₂ gas, CF₄, and CHF₃ and an O₂ gas.

7. The method of ashing a photoresist pattern as set forth in claim 4, wherein the first direct current and the second direct current are independently controlled in

order to control the concentration of the plasma formed in the ashing chamber in accordance with position.

8. The method of ashing a photoresist pattern as set forth in claim 7,
wherein the first current is determined in the range of -10 through 10 A, and
wherein the second current is determined in the range of -10 through 10 A.

9. The method of ashing a photoresist pattern as set forth in claim 4, wherein
the step of removing the photoresist comprises the steps of:

applying power of 100 through $2,500$ W to the bottom electrode; and
maintaining the inner pressure of the ashing chamber in 10 through 600 mT.