

MEMORY DEVICE OR ELECTRONIC DEVICE INCLUDING THE SAME

ABSTRACT OF THE DISCLOSURE

A memory device in which the number of films is reduced. The memory device includes a circuit and a wiring. The circuit includes a first memory cell and a second memory cell. The first memory cell includes a first transistor, a second transistor, and a first capacitor. The second memory cell includes a third transistor, a fourth transistor, and a second capacitor. The second memory cell is stacked over the first memory cell. One of a source and a drain of the first transistor is electrically connected to a gate of the second transistor and the first capacitor. One of a source and a drain of the third transistor is electrically connected to a gate of the fourth transistor and the second capacitor. A gate of the first transistor and a gate of the third transistor are electrically connected to the wiring.

Figure 7