

The invention proposes that the incoming video signal should be underscanned for the purpose of data reduction. Underscanning does indeed entail losses of information. These losses are tolerable, e.g. when reproducing a static picture, when reproducing by means of a small screen or when reproducing a second image in a first image, owing to the necessary reduction ratio which may e.g. be about one-quarter of the main image reproduced.

The luminance and colour difference components, for example, may be selected for processing the video signal. It is possible to use both the same horizontal filter structure and only one analog/digital converter for both parts of the signal (luminance and chrominance), with each of the video signal components being underscanned.

An advantageous example will now be explained with reference to the accompanying drawings, in which:

Fig. 1 is a circuit arrangement for processing video components by means of a multiplexer arrangement, and Fig. 2 is a time graph.

The video signal is applied to the input IN of the circuit arrangement shown in Fig. 1. It is passed to the input of a colour decoder 1, a low pass filter 5 and a synchronous splitting-off circuit and central clock 6. The chrominance signals U, V are applied to the output of the colour decoder 1 and passed to a 2:1 multiplexer 2. The 2:1 multiplexer is switched over at a frequency $FH/8$, which is one-eighth of the line frequency. The V inputs of the multiplexer 2 are thus switched over after every fourth line. The output of the 2:1 multiplexer 2 and the output of the low pass filter 5, to which the luminance signal Y is applied, are passed to a 2:1 multiplexer 3, which is switched over at a frequency $FV/2$. The frequency $FV/2$ corresponds to half the image frequency. The inputs of the multiplexer 3 are thus switched over each time the image is half regenerated. The switchover frequencies $FH/8$, $FV/2$ of the multiplexers 2, 3 are generated by the synchronous splitting-off circuit and central clock 6 and by dividers 7, 8. The output of the multiplexer 3 leads to an analog/digital converter 4, to the output of which the digital data flow is applied.

Fig. 2a shows the line pulses and Fig. 2b the switchover frequency $FH/8$ generated from them by the synchronous splitting-off circuit and central clock 6 and the divider 8. Fig. 2c shows the image pulses and Fig. 2d the switchover frequency $FV/2$ generated from them by the synchronous splitting-off circuit and central clock 6 and the divider 7.

The resultant scanning structure for the video signal is as follows: According to the invention the half-images of a complete image are edited by means of the multiplexers 2, 3, e.g. in such a way that the luminance signal Y is used in the first half and the colour difference signals U and V in the other half.

Thus only the luminance signal Y is passed to the digital/analog converter 4 from incoming image signals for the first half-image.

The next half-image contains only the information of the two colour difference signals U or V, with the first colour component U of the half-image being contained in the first four consecutive lines, and the second component V in the next four consecutive lines. This process is repeated throughout the second half-image.

The two half-images with the following information content are then passed to the input of the analog/digital converter 4:

Lines	1st half-image	2nd half-image
	U	Y
	U	Y
	U	Y
	U	Y
	V	Y
	V	Y
	V	Y
	V	Y
	U	Y
	U	Y
	.	.
	.	.
	.	.

CLAIMS

1. A circuit arrangement for processing video signals comprising chrominance components (U, V) and luminance components (Y), with which, with alternating half-images, only one of the video components at a time is passed on, and which alternately selects one of two parts of the chrominance components (U or V), characterised in that the chrominance component parts (U, V) are passed to a first multiplexer (2), which switches over at a frequency ($FH/8$) lower than the line frequency and which alternately passes on a group of lines of one of the chrominance component parts (U or V), and that the luminance signal (Y) and the output signal from the first multiplexer (2) are passed to a second multiplexer (3), which switches over at half the image frequency ($FV/2$).
2. A circuit arrangement according to claim 1, characterised in that the switch-over frequency ($FH/8$) of the first multiplexer (2) is one eighth of the line frequency.