

Description

BACKGROUND OF THE INVENTION

This invention relates to a semiconductor device fabrication method and device design for suppressing hot carrier effects in MOS integrated circuits and more particularly to a technique for minimizing process-related aging effects in short gate-length MOS-FET devices.

The problems of hot carriers, device aging and reliability have been recognized as one of the major constraints in device scaling. The injection of hot carriers generated by impact ionization in the high drain field region of near-micrometer and submicrometer MOSFET devices degrades the device characteristics. The usual MOSFET processes and device structures, having a gate oxide layer in contact with the silicon substrate over the channel as shown in FIG. 1, are susceptible to hot-carrier trapping at the oxide-silicon interface. The trapped carriers accumulate over time and gradually lead to a shift in threshold voltage of the device that can amount to several tenths of volts or more. This means that circuit design aspects that are affected by gate threshold voltage are susceptible to change over the usual lifetime of circuit usage. In practice, it means that circuits designed with such devices to very close tolerances and initially operative are likely to fail after some period of time. A recent article by Chen et al. entitled "Suppression of Hot-Carrier Effects in Submicrometer CMOS Technology," IEEE Transactions on Electron Devices, Vol. 35, No. 12, Dec. 1988, pages 2210-2219, surveys state-of-the-art approaches to dealing with the problems of hot-carrier aging.

Hot-carrier aging was virtually nonexistent in circuits of MOSFET devices with a gate length of several micrometers. It becomes noticeable as gate length shortens below 2 micrometers and becomes severe at gate lengths of one micrometer and below. Hot carrier generation is caused principally by ionization impact of drain current carriers with the silicon substrate lattice structure in a high electric field. As devices are scaled to smaller size while maintaining a constant drain voltage V_D , the field strength increases. When field strength increases above about 10^5 volt/cm., hot carriers unavoidably begin to be generated. One approach to managing hot carrier effects has been to reduce operating voltages for short gate integrated circuits. Commercial integrated circuit technology uses a standard 5 volts. Reductions to a range of 2.5-3 volts have been proposed to reduce the drain field in submicron circuit technologies. While providing some benefits, this approach leads to further problems of circuit compatibility, reduced performance, and reduced noise immunity. Ultimately, as devices continue to be scaled down, the high field problem returns.

Chen et al. discuss other approaches to control-

ling hot-carrier generation and injection, mostly involving positioning of current path and ionization region to minimize adverse effects. These approaches also are only stop-gap measures which will eventually fail as device sizes continue to be scaled down.

Processing aspects of hot-carrier aging are also considered by Chen et al. It is recognized as being desirable to reduce the number of hot-carrier trapping sites and that trapping at the oxide-silicon interface is the main cause of degradation. Countermeasures include forming and maintaining a high quality oxide layer and seeking to reduce Si-H bond breakage during hot-carrier injection. The latter approach proposes to reduce the hydrogen content of the device structure.

Hydrogen has long been used to fill dangling bonds, forming Si-H at the oxide-silicon interface to minimize the interface states. The Si-H bond can be easily broken by injected hot carriers, however, creating a trapped carrier at the site of the broken bond. It has been suggested to substitute fluorine for hydrogen, or to sinter the devices in a nitrogen atmosphere instead of hydrogen. Chen et al. conclude, however, that it will become necessary to scale down operating voltage to 3.3 volts or below for submicrometer devices.

Another solution to the dangling bond problem was proposed by S. Iwamatsu in Japanese Pat. Appln. (Kokai) 56-125,846, filed March 7, 1980 and published October 2, 1981. At that time, the state of the art in MOSFET technology used gate lengths of several micrometers. Hot carrier aging was not then a problem because hot carriers were not generated in the relatively long gate-length devices of that period. Iwamatsu addresses instead the problem of dangling bonds, explaining that the Si-SiO₂ system has a constant electric charge due to unsaturated bonds at the interface. Because of the presence of interfacial level density Q_{ss} developed at the interface under the influence of this charge, it is difficult to set a low threshold voltage in MOSFET devices. Iwamatsu proposes to implant carbon into the silicon substrate through the gate oxide layer followed by heat treatment in a hydrogen atmosphere. So far as known by applicants, this technique has not been adopted commercially and appears to have given way to the conventional use of hydrogen alone, as discussed above, to saturate silicon bonding locations at the oxide silicon interface. This practice, however, as applied in the current state of the art, turns out to be one of the preconditions for hot-carrier trapping in short gate-length MOS devices.

Accordingly, a need remains for a better technique for suppressing hot-carrier aging in near-micrometer and submicrometer MOSFET devices and the like.

SUMMARY OF THE INVENTION

One object of the invention is to improve long-term reliability of very large-scale integrated (VLSI) circuits without reducing operating drain voltages.

Another object is to reduce hot-carrier aging effects in short-channel MOSFET devices designed and operated in such circuits under conditions in which impact ionization is likely to occur.

A further object of the invention as aforementioned is to minimize time-dependent threshold shift in such devices.

An additional object is to attain the foregoing objects without materially complicating the process for fabrication of such devices and circuits.

The invention is a hot-electron aging-resistant metal-oxide-silicon field effect transistor (MOSFET) and a process for fabrication of such devices in an integrated circuit on a silicon substrate having an upper substrate surface. A gate oxide layer on a first portion of the substrate and forms an oxide-silicon interface at the substrate surface. A conductive gate contact is formed over the gate oxide. Conductive source and drain contacts are formed on second and third portions of the substrate on opposite sides of the gate oxide layer. A channel diffusion of dopant impurities in the first portion of the substrate under the gate oxide defines a threshold voltage of the transistor. Source and drain diffusions of dopant impurities in the second and third portions of the substrate, respectively, are arranged to define a channel length such that hot carriers are generated in the first portion of the silicon substrate under normal operating conditions. In other words, the source and drain diffusions are spaced so that field strength in the channel is at least 10^5 volts per centimeter which is sufficient to create impact ionization producing hot carriers. The first portion of the silicon substrate is doped with carbon atoms in a concentration of at least $10^{16}/\text{cm}^3$ at the silicon-oxide interface, preferably in a concentration range of $10^{16}/\text{cm}^3$ to $10^{20}/\text{cm}^3$ so that trapping of the hot carriers at the interface is suppressed to minimize threshold voltage shift over time.

According to one embodiment of the invention, the carbon atoms are implanted or diffused into a shallow layer of the substrate immediately beneath the substrate surface. In another embodiment, the entire substrate is doped with carbon atoms. The oxide-silicon interface can include hydrogen atoms, in which case a substantial portion of the hydrogen atoms are bonded to carbon atoms. Carbon has a higher bonding strength to hydrogen than does silicon so hot electrons are less likely to dissociate the hydrogen from carbon atoms at the interface and form hot carrier trapping sites.

The invention is most applicable to MOSFET devices in which the channel length is less than 2 micrometers. When the channel length is one micrometer

or less, a device according to the invention built to operate normally at $V_D = V_G = 5.0$ volts has a threshold shift of less than 70 millivolts at an aging time of 24 hours when operated at a drain-to-source voltage V_D of 7.0 volts and a gate voltage V_G of 2.5 volts.

The foregoing and other objects, features and advantages of the invention will become more readily apparent from the following detailed description of a preferred embodiment which proceeds with reference to the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view of a metal-oxide-silicon field effect transistor (MOSFET) illustrating hot carrier effects including hot carrier generation, injection and trapping.

FIG. 2 is a semilogarithmic graph of threshold degradation vs. MOS gate length due to hot carriers.

FIG. 3 is a diagram of an enlargement of a portion of the gate oxide-silicon interface lattice structure of a submicrometer MOSFET device like that of FIG. 1 processed in accordance with the invention.

FIG. 4 is graph of threshold degradation vs. aging time comparing results of examples of submicrometer devices processed in accordance with the invention with results for a control example.

DETAILED DESCRIPTION

The invention can be implemented in an integrated circuit comprising a plurality of metal-oxide-silicon field effect transistor (MOSFET) devices fabricated by otherwise conventional processes, such as that shown in FIG. 1. Although the invention is illustrated in connection with an N-type (NMOS) FET device, it may be used in PMOS FET device technology as well.

Referring to FIG. 1, a near-micrometer or submicrometer N-channel MOSFET device is formed on a P-type silicon substrate 12 having an upper substrate surface 14. A gate oxide layer 16 is conventionally formed, preferably by thermal oxidation, on a first portion of the substrate. The oxide layer contacts the substrate silicon and forms an oxide-silicon interface 18 at the substrate surface. Prior to forming the oxide layer, a channel diffusion is formed, preferably by low-dosage ion implantation of boron dopant impurities, in the first portion of the substrate under the gate oxide. This implant is diffused during thermal oxidation to form the gate oxide and serves to define an initial threshold voltage of the transistor, conventionally set at about 0.7 volts. A conductive gate contact layer 20 is deposited and patterned to overlie the gate oxide. This layer can be formed by depositing, patterning and doping a polysilicon layer, or by metal deposition and patterning. A sidewall spacer 22 is formed on both sides of the gate structure 16, 20, conventionally by deposition and anisotropic reactive ion etching.

The gate structure and sidewall spacer serve as a self-aligning mask for implanting an N-type drain diffusion in an exposed portion of the substrate on one side of the gate structure and a similar source diffusion (not shown) on the opposite side of the gate structure. Optionally, this diffusion can be formed in two steps: first, an N- diffusion 24 prior to forming the sidewall spacer and, second, an N+ diffusion after forming the spacer. These diffusions are preferably formed by ion implantation, with the gate structure alone serving as a mask for the N- implant and the gate structure and spacer serving as a mask for the N+ implant. Subsequent heat treatment diffuses the implants downward and laterally a short distance beneath the gate structure and sidewall spacer.

A conductive (metal, e.g., Al) drain contact 28 is deposited over the exposed portion of the substrate containing the drain diffusion and a similar contact is deposited on an opposite side of the gate oxide layer, both in contact with the substrate silicon surface 14. The final device is conventionally annealed in a hydrogen atmosphere. Hydrogen atoms permeate through the gate structure and bond to dangling silicon bonds at the oxide-silicon interface.

In conventional operation of near-micrometer (less than 2 micrometers) and submicron gate-length devices, a depletion region 30 forms between the N-type and P-type regions of the substrate. When a sufficient positive bias is applied to the gate 20, an inversion layer 32 forms in the P- region, forming an N-type conduction path or channel beneath the gate oxide 16. The spacing between the source and drain diffusions defines a channel length of the MOSFET device. A micrometer-sized device, having a drawn gate length of 1.0 micrometer, typically has an effective channel length of about 0.8 micrometer.

In the context of the present invention, the source and drain diffusions are spaced such that hot carriers 34 (electron and hole pairs) are generated by impact ionization of drain current carriers in a high electric field (field strength at least 10^5 volts per centimeter) region of the channel adjacent the drain diffusion. Some carriers (holes 36) are ejected from the depletion region as a parasitic substrate current I_{sub} . Other carriers are injected into the oxide-silicon interface under the gate oxide layer. In conventional devices, the latter carriers are trapped at the oxide-silicon interface and form cumulative charges of holes 38 and electrons 40. The net cumulative trapped charge eventually becomes dominated by electrons, forming a net potential at the interface which offsets the electric field induced by the potential applied to the gate 20. The net effect is to shift the threshold voltage at which conduction through the inversion channel commences.

In conventional micrometer-sized devices, a threshold voltage initially set at about 0.7 volts will commonly shift by 200 to 300 millivolts over time,

changing the threshold voltage to about 0.9 to 1.0 volts. In a circuit designed efficiently to operate at a drain voltage V_D of 5 volts and a gate voltage V_G of 2.5 volts, this much shift can disrupt proper circuit operation after an aging period that is unacceptably short. This aging period varies, depending on the rate of hot carrier generation, which depends on the drain field being sufficient to cause impact ionization—ultimately a function of gate length.

FIG. 2 shows the dependence of aging (threshold degradation) on MOS gate length after a 24 hour (1445 minutes) period of operation of conventional lightly-doped-drain (LDD) MOSFET devices under standard test conditions of $V_D = 7.0$ volts, $V_G = 2.5$ volts. Data points along the abscissa for gate lengths of 2.5 micrometers and 5 micrometers indicate a threshold shift of less than one millivolt—i.e., below the measurable limits—consistent with experience prior to the advent of short gate-length MOSFET devices. A data point at 2.0 micrometers indicates a threshold shift of one millivolt. From that point, threshold shift increases exponentially as gate length shortens: 33 mV at 1.5 micrometers; 160 mV at 1.0 micrometer; over 800 mV at 0.8 micrometer; and over one volt at 0.6 micrometer.

The present invention greatly reduces hot carrier trapping by reducing trapping sites without materially altering conventional fabrication processing. This is accomplished by doping the first portion of the silicon substrate, which underlies the gate oxide 16, with carbon atoms in a concentration of at least $10^{16}/\text{cm}^3$ at the oxide-silicon interface 18, preferably in a concentration range of $10^{16}/\text{cm}^3$ to $10^{20}/\text{cm}^3$. This has been done two different ways. Both techniques have proven equally successful in suppressing the trapping of the hot carriers at the silicon-oxide interface and minimizing threshold voltage shift over time. In the first approach, carbon atoms are implanted or diffused into a shallow layer of the substrate silicon immediately beneath the substrate surface. This is preferably done prior to forming the oxide layer 16. The second approach simply uses a silicon substrate that is entirely carbon-doped when the crystal from which the wafer is cut is being grown.

FIG. 3 depicts the silicon-oxide interface structure of a MOSFET device when carbon doped in accordance with the invention. Carbon atoms covalently bond in various sites in the silicon lattice 12 near interface 18, and may also persist in sites in the oxide layer 16. Dangling bonds at the oxide-silicon interface are saturated by hydrogen atoms. In conventional devices lacking the carbon atoms, essentially all of the hydrogen atoms would be bonded to silicon atoms and, because of relatively low bond strength, many of the hydrogen-silicon bonds would be disrupted by hot carriers and the hydrogen atoms replaced by a trapped carrier. The bonding strength of carbon to hydrogen is greater than that of silicon, sufficiently so that

nearly all hydrogen atoms are retained at the interface so that trapping sites remain permanently saturated.

FIG. 4 compares aging characteristics over a 24-hour period of three examples of devices made according to the invention with a control example. All four examples were micrometer-sized MOSFET devices made in the same wafer lot, according to the same basic fabrication process steps and conditions except as next described. The control example, for which results are indicated by data points on curve 40, was made without any detectable carbon in the substrate. According to a first example of the invention, wafer 13, for which results are indicated by data points on curve 42, was made with an additional step of shallow (20 KeV) implantation $1E16/cm^3$ carbon atoms into the substrate before forming the gate oxide layer. Wafer 29, for which results are indicated by data points on curve 44, was made as a second example in the same manner as wafer 13 but with a carbon implant dose of $1E20/cm^3$. A third example was made without a separate carbon implantation step but substituted a wafer which was doped with carbon during silicon growth in a concentration of 2.4 parts per million on curve 46. All four examples were tested under the same test conditions: $V_D = 7.0$ volts, $V_G = 2.5$ volts. These conditions are more severe than the usual operating conditions for such devices, which were designed to operate at $V_D = V_G = 5.0$ volts.

The curve 40 for the control example exhibits a typical characteristic of hot carrier aging of conventional short-channel MOSFET devices. It rises sharply at first (200 millivolts in 1,000 minutes) and then gradually decreases in slope in a rising exponential curve as hot electron trapping sites are filled. At the end of 24 hours, the threshold shift for the control is 240 millivolts.

All three examples according to the invention exhibit aging characteristics that are quite similar to one another but strikingly different from that of the control example. Threshold shift occurs more gradually, no more than 10 millivolts after five hours, 30 millivolts in 15 hours, and 60 millivolts in 24 hours. In continued operation over a longer period, threshold shift of such devices levels off at about 75-100 millivolts. With optimization of the process according to the invention, further reductions in threshold shift are expected.

Having illustrated and described the principles of our invention in a preferred embodiment thereof, it should be readily apparent to those skilled in the art that the invention can be modified in arrangement and detail without departing from such principles.

Claims

1. An integrated circuit having a hot-electron aging-resistant metal-oxide-silicon field effect transis-

tor (MOSFET), said transistor comprising:

a silicon substrate (12) having an upper substrate surface (14);

a gate oxide layer (16) covering a first portion of the substrate and forming an oxide-silicon interface (18) at the substrate surface;

a conductive gate contact (20) overlying the gate oxide;

a conductive source contact (28) covering a second portion of the substrate on one side of the gate oxide layer;

a conductive drain contact covering a third portion of the substrate on an opposite side of the gate oxide layer;

a channel diffusion of dopant impurities in the first portion of the substrate under the gate oxide defining a threshold voltage of the transistor;

source and drain diffusions (24, 26) of dopant impurities in the second and third portions of the substrate, respectively;

the diffusions being arranged to define a channel length such that, in use, the field strength in the channel is at least 10^5 volts/cm, whereby hot carriers are generated by impact ionization in the first portion of the silicon substrate; and

the first portion of the silicon substrate being doped with carbon atoms in a concentration of at least $10^{16}/cm^3$ at the interface (18) so that trapping of the hot carriers at the interface is suppressed and a shift in the threshold voltage over time is minimized.

2. The integrated circuit according to claim 1 in which the first portion of the silicon substrate is doped with carbon atoms in a concentration range of $10^{16}/cm^3$ to $10^{20}/cm^3$.
3. The integrated circuit according to claim 1 or 2 in which the source and drain diffusions are spaced so that the channel length is less than 2 micrometers.
4. The integrated circuit according to claim 1, 2 or 3 in which the carbon atoms are implanted or diffused into a shallow layer of the substrate immediately beneath the substrate surface.
5. The integrated circuit according to claim 1, 2 or 3 in which the entire substrate is doped with said carbon atoms.
6. The integrated circuit according to any preceding claim in which the oxide-silicon interface includes hydrogen atoms, a portion of which are bonded to carbon atoms.



nearly all hydrogen atoms are retained at the interface so that trapping sites remain permanently saturated.

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All three examples according to the invention exhibit aging characteristics that are quite similar to one another but strikingly different from that of the control example. Threshold shift occurs more gradually, no more than 10 millivolts after five hours, 30 millivolts in 15 hours, and 60 millivolts in 24 hours. In continued operation over a longer period, threshold shift of such devices levels off at about 75-100 millivolts. With optimization of the process according to the invention, further reductions in threshold shift are expected.

Having illustrated and described the principles of our invention in a preferred embodiment thereof, it should be readily apparent to those skilled in the art that the invention can be modified in arrangement and detail without departing from such principles.

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tor (MOSFET), said transistor comprising:

a silicon substrate (12) having an upper substrate surface (14);

a gate oxide layer (16) covering a first portion of the substrate and forming an oxide-silicon interface (18) at the substrate surface;

a conductive gate contact (20) overlying the gate oxide;

a conductive source contact (28) covering a second portion of the substrate on one side of the gate oxide layer;

a conductive drain contact covering a third portion of the substrate on an opposite side of the gate oxide layer;

a channel diffusion of dopant impurities in the first portion of the substrate under the gate oxide defining a threshold voltage of the transistor;

source and drain diffusions (24, 26) of dopant impurities in the second and third portions of the substrate, respectively;

the diffusions being arranged to define a channel length such that, in use, the field strength in the channel is at least 10^5 volts/cm, whereby hot carriers are generated by impact ionization in the first portion of the silicon substrate; and

the first portion of the silicon substrate being doped with carbon atoms in a concentration of at least $10^{16}/cm^3$ at the interface (18) so that trapping of the hot carriers at the interface is suppressed and a shift in the threshold voltage over time is minimized.

2. The integrated circuit according to claim 1 in which the first portion of the silicon substrate is doped with carbon atoms in a concentration range of $10^{16}/cm^3$ to $10^{20}/cm^3$.
3. The integrated circuit according to claim 1 or 2 in which the source and drain diffusions are spaced so that the channel length is less than 2 micrometers.
4. The integrated circuit according to claim 1, 2 or 3 in which the carbon atoms are implanted or diffused into a shallow layer of the substrate immediately beneath the substrate surface.
5. The integrated circuit according to claim 1, 2 or 3 in which the entire substrate is doped with said carbon atoms.
6. The integrated circuit according to any preceding claim in which the oxide-silicon interface includes hydrogen atoms, a portion of which are bonded to carbon atoms.



7. The integrated circuit according to any preceding claim in which the source and drain diffusions are spaced so that the channel length is one micrometer or less.
8. An integrated circuit fabrication process for making a hot-electron aging-resistant metal-oxide-silicon field effect transistor (MOSFET) comprising:
 - providing a silicon substrate (12) having an upper substrate surface (14);
 - forming a gate oxide layer (16) over a first portion of the substrate with an oxide-silicon interface (18) at the substrate surface;
 - forming a conductive gate contact (20) over the gate oxide;
 - forming a conductive source contact over a second portion of the substrate on one side of the gate oxide layer and a conductive drain contact (28) over a third portion of the substrate on an opposite side of the gate oxide layer;
 - forming a channel diffusion in the first portion of the substrate under the gate oxide to define a threshold voltage of the transistor and source and drain diffusions (24, 26) in the second and third portions of the substrate, respectively;
 - arranging the diffusions to define a channel length such that, in use, the field strength in the channel is at least 10^5 volts/cm, whereby hot carriers are generated by impact ionization in the first portion of the silicon substrate; and
 - doping the first portion of the silicon substrate with carbon atoms in a concentration of at least $10^{16}/\text{cm}^3$ at the interface (18) so that trapping of the hot carriers at the interface is suppressed and a shift in the threshold voltage over time is minimized.
9. The integrated circuit process according to claim 10 in which the first portion of the silicon substrate is doped with carbon atoms in a concentration range of $10^{16}/\text{cm}^3$ to $10^{20}/\text{cm}^3$.
10. The integrated circuit process according to claim 8 or 9 including spacing the source and drain diffusions so that the channel length is less than 2 micrometers.
11. The integrated circuit process according to claim 8, 9 or 10 including spacing the source and drain diffusions so that the channel length is one micrometer or less.
12. The integrated circuit device according to any of claims 8-11 in which the doping step includes implanting or diffusing the carbon atoms into a shallow layer of the substrate immediately beneath the substrate surface.

13. The integrated circuit process according to any of claims 8-11 in which the doping step includes providing as said substrate a silicon wafer, the entirety of which is doped with carbon atoms.

14. The integrated circuit process according to any of claims 8-13 in which hydrogen atoms in the oxide-silicon interface are bonded to carbon atoms.

15. The integrated circuit process according to any of claims 8-14 including spacing the source and drain diffusions so that the channel length is one micrometer or less.

Patentansprüche

1. Eine integrierte Schaltung mit einem gegenüber der Alterung durch heiße Elektronen resistenten Metall-Oxid-Silizium-Feldeffekttransistor (MOSFET), wobei der Transistor folgende Merkmale aufweist:
 - ein Siliziumsubstrat (12) mit einer oberen Substratoberfläche (14);
 - eine Gate-Oxidschicht (16), die einen ersten Abschnitt des Substrats bedeckt und eine Oxid-Silizium-Grenzfläche (18) an der Substratoberfläche bildet;
 - einen leitfähigen Gate-Kontakt (20), der über dem Gate-Oxid liegt;
 - einen leitfähigen Source-Kontakt (28), der einen zweiten Abschnitt des Substrats auf einer Seite der Gate-Oxidschicht bedeckt;
 - einen leitfähigen Drain-Kontakt, der einen dritten Abschnitt des Substrats auf einer gegenüberliegenden Seite der Gate-Oxidschicht bedeckt;
 - eine Kanaldiffusion von Dotierungsstörstellen in dem ersten Abschnitt des Substrats unter das Gate-Oxid, die eine Schwellenspannung des Transistors festlegt;
 - Source- und Drain-Diffusionen (24, 26) von Dotierungsstörstellen in den zweiten bzw. dritten Abschnitt des Substrats;
 - wobei die Diffusionen eingerichtet sind, um eine Kanallänge derart zu bestimmen, daß bei der Verwendung, bei der die Feldstärke in dem Kanal mindestens 10^5V/cm beträgt, heiße Träger durch Stoßionisation in dem ersten Abschnitt des Siliziumsubstrats erzeugt werden; und wobei der erste Abschnitt des Siliziumsubstrats mit Kohlenstoffatomen in einer Konzentration von mindestens $10^{16}/\text{cm}^3$ an der Grenzfläche (18) dotiert ist, so daß ein Einfangen der heißen Träger an der Grenzfläche unterdrückt wird und eine Verschiebung der Schwellenspannung mit fortschreitender Zeit minimiert ist.
2. Die integrierte Schaltung gemäß Anspruch 1, bei der der erste Abschnitt des Siliziumsubstrats mit



Kohlenstoffatomen in einem Konzentrationsbereich von $10^{16}/\text{cm}^3$ bis $10^{20}/\text{cm}^3$ dotiert ist.

3. Die integrierte Schaltung gemäß Anspruch 1 oder 2, bei der die Source- und Drain-Diffusionen derart beabstandet sind, daß die Kanallänge kleiner als 2 Mikrometer ist.
4. Die integrierte Schaltung gemäß Anspruch 1, 2 oder 3, bei der die Kohlenstoffatome in eine flache Schicht des Substrats unmittelbar unter der Substratoberfläche implantiert oder diffundiert sind.
5. Die integrierte Schaltung gemäß Anspruch 1, 2 oder 3, bei der das gesamte Substrat mit den Kohlenstoffatomen dotiert ist.
6. Die integrierte Schaltung gemäß einem beliebigen vorhergehenden Anspruch, bei der die Oxid-Silizium-Grenzfläche Wasserstoffatome einschließt, wobei ein Teil derselben mit Kohlenstoffatomen gebunden ist.
7. Die integrierte Schaltung gemäß einem beliebigen vorhergehenden Anspruch, bei der die Source- und Drain-Diffusionen derart beabstandet sind, daß die Kanallänge einen Mikrometer oder kleiner ist.
8. Ein Herstellungsverfahren für eine integrierte Schaltung zum Herstellen eines gegen Alterung durch heiße Elektronen resistenten Metall-Oxid-Silizium-Feldeffekttransistors (MOSFET), das folgende Merkmale aufweist:
Vorsehen eines Siliziumsubstrats (12) mit einer oberen Substratoberfläche (14);
Bilden einer Gate-Oxidschicht (16) über einem ersten Abschnitt des Substrats mit einer Oxid-Silizium-Grenzfläche (18) an der Substratoberfläche;
Bilden eines leitfähigen Gate-Kontakts (20) über dem Gate-Oxid;
Bilden eines leitfähigen Source-Kontakts über einem zweiten Abschnitt des Substrats auf einer Seite der Gate-Oxidschicht und eines leitfähigen Drain-Kontakts (28) über einen dritten Abschnitt des Substrats auf einer gegenüberliegenden Seite der Gate-Oxidschicht;
Bilden einer Kanaldiffusion in dem ersten Abschnitt auf dem Substrat unter dem Gate-Oxid, um eine Schwellenspannung des Transistors festzulegen, und von Source- und Drain-Diffusionen (24, 26) in dem zweiten bzw. dritten Abschnitt des Substrats;
Einrichten der Diffusionen, um eine Kanallänge derart zu bestimmen, daß bei der Verwendung, bei der die Feldstärke in dem Kanal mindestens

10^5V/cm beträgt, heiße Träger durch Stoßionisation in dem ersten Abschnitt des Siliziumsubstrats erzeugt werden; und

Dotieren des ersten Abschnitts des Siliziumsubstrats mit Kohlenstoffatomen in einer Konzentration von mindestens $10^{16}/\text{cm}^3$ an der Grenzfläche (18), so daß ein Einfangen der heißen Träger an der Grenzfläche unterdrückt wird und eine Verschiebung der Schwellenspannung mit fortschreitender Zeit minimiert wird.

9. Das Verfahren für integrierte Schaltungen gemäß Anspruch 10, bei dem der erste Abschnitt des Siliziumsubstrats mit Kohlenstoffatomen in einem Konzentrationsbereich von $10^{16}/\text{cm}^3$ bis $10^{20}/\text{cm}^3$ dotiert wird.
10. Das Verfahren für integrierte Schaltungen gemäß Anspruch 8 oder 9, das das Beabstanden der Source- und Drain-Diffusionen einschließt, so daß die Kanallänge zwei Mikrometer oder geringer ist.
11. Das Verfahren für integrierte Schaltungen gemäß Anspruch 8, 9 oder 10, das das Beabstanden der Source- und Drain-Diffusionen einschließt, so daß die Kanallänge ein Mikrometer oder geringer ist.
12. Das Verfahren für integrierte Schaltungen gemäß einem beliebigen der Ansprüche 8 bis 11, bei dem der Dotierungsschritt das Implantieren oder Diffundieren der Kohlenstoffatome in eine flache Schicht des Substrats unmittelbar unter der Substratoberfläche einschließt.
13. Das Verfahren für integrierte Schaltungen gemäß einem beliebigen der Ansprüche 8 bis 11, bei dem der Dotierungsschritt das Vorsehen eines Siliziumwafers als das Substrat einschließt, wobei die Gesamtheit desselben mit Kohlenstoffatomen dotiert wird.
14. Das Verfahren für integrierte Schaltungen gemäß einem beliebigen der Ansprüche 8 bis 13, bei dem Wasserstoffatome in der Oxid-Silizium-Grenzfläche mit Kohlenstoffatomen gebunden sind.
15. Das Verfahren für integrierte Schaltungen gemäß einem beliebigen der Ansprüche 8 bis 14, das das Beabstanden der Source- und Drain-Diffusionen einschließt, so daß die Kanallänge ein Mikrometer oder geringer ist.



Revendications

1. Circuit intégré comportant un transistor à effet de champ métal-oxyde-silicium (MOSFET) résistant contre le vieillissement par électrons chauds, ledit transistor comprenant:
 - un substrat de silicium (12) comportant une surface supérieure de substrat (14);
 - une couche d'oxyde de grille (16) recouvrant une première partie du substrat et constituant une interface oxyde-silicium (18) à la surface du substrat;
 - un contact de grille conducteur (20) recouvrant l'oxyde de grille;
 - un contact de source conducteur (28) recouvrant une seconde partie du substrat sur un côté de la couche d'oxyde de grille;
 - un contact de drain conducteur recouvrant une troisième partie du substrat sur le côté opposé de la couche d'oxyde de grille;
 - une diffusion de canal d'impuretés de dopant, dans la première partie du substrat, sous l'oxyde de grille, définissant la tension de seuil du transistor;
 - des diffusions de source et de drain (24, 26) d'impuretés de dopant respectivement dans les seconde et troisième parties du substrat;
 - les diffusions étant aménagées de façon à définir une longueur de canal telle que lors de l'utilisation, l'intensité de champ dans le canal est au moins de 10^5 volts/cm, ce par quoi des porteurs chauds sont générés par ionisation d'impact dans la première partie du substrat de silicium; et
 - la première partie du substrat de silicium étant dopée avec des atomes de carbone selon une concentration au moins de 10^{16} /cm³ à l'interface (18), de sorte que le piégeage des porteurs chauds soit supprimé à l'interface, et que le décalage de la tension de seuil soit minimisé dans le temps.
2. Circuit intégré selon la revendication 1, dans lequel la première partie du substrat de silicium est dopée avec des atomes de carbone selon une plage de concentration de 10^{16} /cm³ à 10^{20} /cm³.
3. Circuit intégré selon la revendication 1 ou 2, dans lequel les diffusions de source et de drain sont espacées de façon que la longueur du canal soit inférieure à 2 micromètres.
4. Circuit intégré selon la revendication 1, 2 ou 3, dans lequel les atomes de carbone sont implantés ou diffusés dans une couche du substrat peu profonde, située juste en-dessous de la surface du substrat.
5. Circuit intégré selon la revendication 1, 2 ou 3, dans lequel l'intégralité du substrat est dopé avec lesdits atomes de carbone.
6. Circuit intégré selon l'une quelconque des revendications précédentes, dans lequel l'interface oxyde-silicium contient des atomes d'hydrogène, dont une partie est liée aux atomes de carbone.
7. Circuit intégré selon l'une quelconque des revendications précédentes, dans lequel les diffusions de source et de drain sont espacées de façon que la longueur de canal soit de un micromètre ou moins.
8. Procédé de fabrication de circuit intégré pour réaliser un transistor à effet de champ métal-oxyde-silicium (MOSFET) résistant contre le vieillissement par électrons chauds, comprenant:
 - la réalisation d'un substrat en silicium (12) comportant une surface supérieure de substrat (14);
 - la réalisation d'une couche d'oxyde de grille (16) au-dessus d'une première partie du substrat, avec une interface oxyde-silicium (18) à la surface du substrat;
 - la formation d'un contact de grille conducteur (20) au-dessus de l'oxyde de grille;
 - la formation d'un contact de source conducteur au-dessus d'une seconde partie du substrat sur un côté de la couche d'oxyde de grille et d'un contact de drain conducteur (28) au-dessus d'une troisième partie du substrat sur le côté opposé de la couche d'oxyde de grille;
 - la formation d'une diffusion de canal dans la première partie du substrat, sous l'oxyde de grille, définissant la tension de seuil du transistor et de diffusions de source et de drain (24, 26) respectivement dans les seconde et troisième parties du substrat;
 - l'aménagement des diffusions de façon à définir une longueur de canal telle que, lors de l'utilisation, l'intensité du champ dans le canal soit au moins de 10^5 volts/cm, ce par quoi des porteurs chauds sont générés par ionisation d'impact dans la première partie du substrat de silicium; et
 - le dopage de la première partie du substrat de silicium avec des atomes de carbone selon une concentration au moins de 10^{16} /cm³ à l'interface (18), de sorte que le piégeage des porteurs chauds soit supprimé à l'interface, et que le décalage de la tension de seuil soit minimisé dans le temps.
9. Procédé pour circuit intégré selon la revendication 8, dans lequel la première partie du substrat de silicium est dopée avec des atomes de carbo-



ne selon une plage de concentration de 10^{18} /cm³ à 10^{20} /cm³.

10. Procédé pour circuit intégré selon la revendication 8 ou 9, comportant un espacement des diffusions de source et de drain tel que la longueur du canal soit inférieure à 2 micromètres. 5
11. Procédé pour circuit intégré selon la revendication 8, 9 ou 10, comportant un espacement des diffusions de source et de drain tel que la longueur du canal soit de 1 micromètre ou moins. 10
12. Procédé de circuit intégré selon l'une quelconque des revendications 8 à 11, dans lequel l'étape de dopage comporte l'implantation ou la diffusion des atomes de carbone dans une couche de substrat peu profonde, située juste en-dessous de la surface du substrat. 15
13. Procédé pour circuit intégré selon l'une quelconque des revendications 8 à 11, dans lequel l'étape de dopage comporte la réalisation en tant que dit substrat, d'une tranche de silicium, dont l'intégralité est dopée avec les atomes de carbone. 20
14. Procédé pour circuit intégré selon l'une quelconque des revendications 8 à 13, dans lequel des atomes d'hydrogène situés dans l'interface oxydesilicium sont liés aux atomes de carbone. 25
15. Procédé pour circuit intégré selon l'une quelconque des revendications 8 à 14, comportant un espacement des diffusions de source et de drain tel que la longueur de canal soit de un micromètre ou moins 30

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