

What is claimed is:

1. A vertical memory device, comprising:

a gate structure including a first gate electrode on a peripheral circuit region of a substrate, the substrate containing a cell region and the peripheral circuit region;

a plurality of second gate electrodes sequentially stacked on the cell region of the substrate, the plurality of second gate electrodes spaced apart from each other in a vertical direction to an upper surface of the substrate;

a channel extending in the vertical direction on the cell region of the substrate and extending through at least one of the second gate electrodes; and

a first insulating interlayer covering the gate structure on the peripheral circuit region of the substrate, a cross-section in one direction of an upper surface of a portion of the first insulating interlayer overlapping the gate structure in the vertical direction having a shape of a portion of a polygon and wherein the upper surface of the portion of the first insulating interlayer overlapping the gate structure in the vertical direction is not flat.

2. The vertical memory device of claim 1, further comprising:

a second insulating interlayer on the first insulating interlayer,

wherein a cross-section in the direction of an upper surface of a portion of the second insulating interlayer has a curved shape corresponding to that of the upper surface of the portion of the first insulating interlayer.

3. The vertical memory device of claim 2, wherein the first and second insulating interlayers include high density plasma (HDP) oxide and TEOS, respectively.

4. The vertical memory device of claim 2 or claim 3, further comprising:
a third insulating interlayer on the second insulating interlayer,
wherein the third insulating interlayer has a flat upper surface.

5. The vertical memory device of claim 4, wherein the second and third insulating interlayers include substantially the same material.

6. The vertical memory device of claim 1, wherein the second gate electrodes include third to fifth gate electrodes sequentially stacked on the substrate in the vertical direction, and
wherein the first insulating interlayer is also on the cell region of the substrate to cover the third gate electrode.

7. The vertical memory device of claim 6, further comprising:
a second insulating interlayer formed between the first insulating interlayer and the fourth gate electrode.

8. The vertical memory device of claim 7, wherein the first and second insulating interlayers include high density plasma (HDP) oxide and TEOS, respectively.

9. The vertical memory device of claim 7 or claim 8, wherein an upper surface of a portion of each of the first and second insulating interlayers has a concave shape on the cell region of the substrate.

10. The vertical memory device of claim 9, wherein the concave portion of the

upper surface of the first insulating interlayer has a cross-section in the direction having a shape of a portion of a polygon, and the concave portion of the upper surface of the second insulating interlayer has a cross-section in the direction with a curved shape corresponding to the shape of the cross-section of the concave portion of the upper surface of the first insulating interlayer.

11. The vertical memory device of any one of claims 6 to 10, wherein one or ones of the fourth gate electrodes have a concave portion.

12. The vertical memory device of any one of claims 6 to 11, wherein the third, the fourth and the fifth gate electrodes serve as a ground selection line (GSL), a word line, and a string selection line (SSL), respectively.

13. A vertical memory device, comprising:

- a gate structure including a first gate electrode on a peripheral circuit region of a substrate, the substrate containing a cell region and the peripheral circuit region;
- a second gate electrode on the cell region of the substrate;
- a first insulating interlayer on the cell region and the peripheral circuit region of the substrate, the first insulating interlayer covering the gate structure and the second gate electrode;
- a second insulating interlayer on the first insulating interlayer;
- third and fourth gate electrodes sequentially stacked on a portion of the second insulating interlayer on the cell region of the substrate, the third and fourth gate electrodes spaced apart from each other in a vertical direction to an upper surface of the substrate; and
- a channel extending through the third and fourth gate electrodes in the vertical

direction,

wherein an upper surface of at least a portion of the first insulating interlayer on the peripheral circuit region of the substrate has an angular protrusion and depression shape; and

wherein an upper surface of a portion of the first insulating interlayer overlapping the gate structure in the vertical direction is not flat.

14. The vertical memory device of claim 13, wherein an upper surface of the portion of the second insulating interlayer on the peripheral circuit region of the substrate has a rounded protrusion and depression shape corresponding to the shape of the upper surface of the at least a portion of the first insulating interlayer.

15. The vertical memory device of claim 13 or claim 14, wherein the first and second insulating interlayers include high density plasma (HDP) oxide and TEOS, respectively.

16. The vertical memory device of any one of claims 13 to 15, further comprising:

a third insulating interlayer covering the third and fourth gate electrodes on the second insulating interlayer,

wherein the third insulating interlayer has a flat upper surface.

17. The vertical memory device of any one of claims 13 to 16, wherein the second, the third, and the fourth gate electrodes serve as a ground selection line (GSL), a word line, and string selection line (SSL), respectively.

18. A vertical memory device, comprising:

a gate structure including a first gate electrode on a peripheral circuit region of a substrate, the substrate containing a cell region and the peripheral circuit region;

a plurality of second gate electrodes sequentially stacked on the cell region of the substrate, the plurality of second gate electrodes spaced apart from each other in a vertical direction to an upper surface of the substrate;

a channel extending through at least one of the second gate electrodes in the vertical direction on the cell region of the substrate; and

first to third insulating interlayers sequentially stacked on the peripheral circuit region of the substrate,

wherein the first insulating interlayer covers the gate structure, and an upper surface of at least a portion of the first insulating interlayer has an angular protrusion and depression shape,

wherein an upper surface of a portion of the second insulating interlayer has a rounded protrusion and depression shape corresponding to that of the upper surface of the at least a portion of the first insulating interlayer, and

wherein the third insulating interlayer has a flat upper surface.

19. The vertical memory device of claim 18, wherein the second and third insulating interlayers include substantially the same material, which is different from a material of the first insulating interlayer.

20. The vertical memory device of claim 18 or claim 19, wherein the second gate electrodes include third to fifth gate electrodes sequentially stacked in the vertical

direction on the substrate, and

wherein the first and second insulating interlayers are also on the cell region of the substrate, such that the first insulating interlayer covers the third gate electrode, and the second insulating interlayer is between the first insulating interlayer and the fourth gate electrode.