SEMICONDUCTOR MEMORY DEVICE

The present invention relates to semiconductor memory devices, for example an erasable programmable ROM (or 'EPROM').

In general, in EPROMs, a memory cell portion and a peripheral circuit portion are constructed of N-channel type metal-insulator-semiconductor field effect transistors (hereinbelow, termed "MISFETs") in order to attain a high operating speed and a high packaging density. In order to reduce current consumption, the inventors decided to try to form the peripheral circuit portion of complementary metal-oxide-semiconductor field effect transistors (hereinbelow termed "CMOS"). It has been found, however, that a problem is posed by the mere use of CMOS, as will now be described.

A common P-type well is formed in an N-type semiconductor substrate, and N-channel MISFETs are respectively disposed within the P-type well. A contact region for grounding the well is provided, and because of the wiring between the various elements, the contact region is inevitably arranged in a peripheral part of the well. Accordingly, the distance between an element and the contact region is rather long. For this reason, holes emitted from a transistor drain region into the well during operation have to pass through a relatively high resistance to reach the contact region, and the resulting voltage drop component raises the potential of

the well, especially in a portion to which a high voltage (21 V or 25 V for writing) is applied. In these circumstances, a P-N-P-N thyristor structure formed of the drain (N-type), the P-type well, the N-type substrate, and a P^+-type diffusion region in a P-channel element of the CMOS structure is triggered by the rise of the well potential and is turned "on". It was feared that so-called latch-up would occur and cause breakdown of the element.

As a countermeasure, the inventors considered attaining a high breakdown voltage by adopting an offset gate in the CMOS structure and disposing a low concentration (N^--type or P^--type) region adjacent to each drain region. In this case, however, the manufacturing process becomes undesirably complicated because such low concentration regions need to be formed separately. Moreover, the drains of the MISFETs within the well, in particular, have 21 V (in the writing mode) and 5 V (in the reading mode) applied thereto, and well potential accordingly changes between 21 V and 5 V, so that the writing - reading switching operation becomes unstable.

Further, in the CMOS structure described above it is necessary to provide a significant distance between the walls and between the wells and the diffused region. This is a drawback for high packaging density and reduced chip size.

In a first aspect, the invention provides a semiconductor memory device comprising:

a P-type semiconductor body;

a memory cell portion which includes a plurality of non-volatile memory cells formed in a part of said semiconductor body; and

a peripheral circuit portion which is formed in parts of said semiconductor body that are not provided with said non-volatile memory cells and which includes a first circuit portion made of circuit elements arranged to be energized by a first voltage and a second circuit portion made of circuit elements arranged to be energized by a second voltage lower than said first voltage;

said circuit elements of said first circuit portion being first insulated gate type FETs which have N-type channels and, are formed directly in the semiconductor body while said circuit elements of said second circuit portion are a plurality of pairs of second insulated gate type FETs, each of which pairs comprises a P-channel FET and an N-channel FET.

In a second aspect there is provided a method of manufacturing embodiments of the invention comprising:

the step of forming a field insulating film on selected areas of one major surface of a P-type semiconductor body, said field insulating film isolating said one major surface of said semiconductor body into at least first, second and third areas;

the step of forming an N-type well region in a part

of said first area so as to leave a body region in another part of said first area;

the step of forming a first polycrystalline silicon layer on said three areas, and selectively removing said first polycrystalline layer to leave a plurality of gate electrodes on said second area and a first polycrystalline silicon film on said third area;

the step of forming an insulating film on the surfaces of said plurality of gate electrodes and said first polycrystalline silicon film respectively formed on said second area and said third area;

the step of forming a second polycrystalline silicon layer on the first, second and third areas;

the step of selectively removing said second polycrystalline silicon layer and said first polycrystalline silicon film to form a plurality of gate electrodes on said well and body regions of said first area and to form gate electrodes of non-volatile memory cells on said third area,

the step of introducing an N-type impurity into said body region of said first area, and said second and third areas by using as a mask said plurality of gate electrodes formed on said body region of said first area and on said second and third areas, thereby to form a plurality of N-type semiconductor regions;

the step of introducing a P-type impurity into said well region of said first area by using as a mask said gate electrode formed on said well region;

the step of forming an insulating film on said first, second and third areas and selectively removing this insulating film, thereby to form contact holes; and

the step of forming wiring leads which connect with said plurality of semiconductor regions through said contact holes.

Embodiments of the present invention will now be described, in detail, by way of example, with reference to the accompanying drawings in which:

Figure 1 is a partial block diagram of a first embodiment of the present invention;

Figure 2 is a partial equivalent circuit diagram of the first embodiment;

Figure 3 is a partial sectional view of memory cell and peripheral circuit portions of the first embodiment;

Figure 4 is a partial sectional view of the high-voltage circuit of a second embodiment;

Figures 5A to 5I are partial sectional views of stages in one method of the manufacture of the first embodiment;

Figures 6A to 6C are partial sectional views of principal stages in one method of the manufacture of the second embodiment.

Figure 1 shows a block diagram of the essential circuits which are arranged on the chip of an EPROM. Selection signals from an address buffer AB are respectively supplied to memory cells M-CEL through an X-decoder X-DEC and a Y-decoder Y-DEC. In addition, input signals from or output signals to an input/output buffer IOB are supplied thereto or therefrom through a writing circuit WC or a sense amplifier SA. To be noted here is that the respective decoders X-DEC and Y-DEC, sense amplifier SA and input/output buffer IOB to which low voltages approximately equal to a reading voltage (5 V) are applied are constructed of the CMOS described before, and that the writing circuit WC to which a high voltage (21 V or 25 V) is applied is entirely constructed of N-channel MISFETs which are disposed in a P-type substrate

itself.

Figure 2 shows partial equivalent circuits of the respective decoders, the memory cell portion, the writing circuit and the input/output buffer of the EPROM shown in Figure 1. Here, the "writing circuit" is equivalent to a high voltage application circuit to which the writing voltage V_{PP} is applied. The portion to which the reading voltage V_{CC} is applied is distinguished as a reading voltage application circuit from the writing voltage system.

Referring to Figure 2, memory cells are formed of N-channel MISFETs (Q_{M1-1}, ... Q_{M1-n}) - (Q_{Mm-1}, ... Q_{Mm-n}) in the vertical and horizontal directions, the N-channel MISFETs having a dual gate structure which consists of a floating gate and a control gate. Common word lines W_1, ... W_m which couple the control gates, and common bit lines D_1, ... D_n which couple the drains of the MISFETs are intersectingly arranged in the form of a matrix. Each word line is connected, at one end, to the X-decoder X-DEC through a transfer gate of the depletion mode Q_{T1}, ... or Q_{Tm}, and at the other end, to a power source terminal V_{PP} through a high resistance element R_1, ... or R_m constituting a pull-up circuit for charging the word line. The respective bit lines are connected to the writing circuit WC and the input/output buffer IOB through switching MISFETs Q_{S1}, ... and Q_{Sm} and by a common bit line. In addition, the gates of the FETs Q_{S1}, ... and Q_{Sm} are

respectively connected to the Y-decoder Y-DEC through transfer gates of the depletion mode Q_{T1}', ... and Q_{Tm}'. Further, at the intermediate positions between the switching FETs Q_{S1}, ... Q_{Sm} and the transfer gate MISFETs Q_{T1}', ... Q_{Tm}', high resistance elements R_1', ... R_m' constituting a pull-up circuit are connected between these positions and the power source terminal V_{PP}. The X-decoder X-DEC is constructed of a plurality of pairs each consisting of a P-channel MISFET Q_6 and an N-channel MISFET Q_7. On the other hand, the Y-decoder Y-DEC is constructed of a plurality of pairs each consisting of a P-channel MISFET Q_8 and an N-channel MISFET Q_9. Further, the input/output buffer IOB is similarly constructed of a pair consisting of a P-channel MISFET Q_4 and an N-channel MISFET Q_5. The low voltage is applied to the X-decoder X-DEC, Y-decoder Y-DEC and the input/output buffer IOB mentioned above. In addition, the writing circuit is constructed of N-channel MISFETs Q_1, Q_2 and Q_3, among which the MISFET Q_2 is of the depletion mode. The high voltage is applied to the circuit constructed of such MISFETs of the single channel.

Referring now to Figure 3, the construction of the principal portions according to the present embodiment will be described. This figure shows a section of a part of the memory cell portion M-CEL together with sections of the respective MISFETs Q_1, Q_2 and Q_3, and Q_4 and Q_5 of the writing circuit and the input/output buffer shown in Figure 2.

The respective element areas are isolated by field SiO_2 films 2 provided on one major surface of a common P-type silicon substrate 1, and the corresponding MISFETs are formed within the respective element areas. It is a characterizing feature that, particularly in the peripheral circuit portion, the high voltage system to which the writing voltage is applied is entirely constructed of N-channel MISFETs, which the low voltage system to which the reading voltage is applied is constructed of CMOS including an N-type well 3. Regarding the MISFETs Q_1 - Q_3 of the high voltage system, and N^+-type source region 4 of Q_1 is connected to the sense amplifier SA, the high voltage V_{PP} is applied to an N^+-type drain region 5 common to Q_1 and Q_2, and Q_2 is made to operate in the depletion mode by an impurity doping layer 6 in a channel portion. The other N^+-type diffusion region 7 of Q_2 is common to Q_3, and an N^+-type source region 8 of Q_3 is grounded. Gate electrodes 9, 10 and 11 of the respective FETs Q_1 - Q_3 are all formed of a first layer of polycrystalline silicon (hereinbelow, termed "poly-Si"). Numerals 12, 13, 14 and 15 indicate aluminum electrodes or wiring leads. Likewise, numeral 16 indicates a gate oxide film, numeral 17 a surface oxide film of a poly-Si film, and numeral 18 a phospho-silicate glass film.

On the other hand, the input buffer of the low voltage system is made of CMOS which consists of the N-

channel MISFET Q_5 and the P-channel MISFET Q_4. An N^+-type source region 19 of Q_5 is grounded, and an N^+-type drain region 20 thereof is connected with a P^+-type diffusion region 21 of Q_4 by an aluminum wiring lead 22. The other P^+ -type region 23 of Q_4 is connected to a low voltage source together with an N^+ -type feeding region 24 of the well 3. Respecitve gate electrodes 25 and 26 of both the FETs Q_4 and Q_5 are formed of a second layer of poly-Si, and are interconnected. Likewise to numeral 22, numerals 27, 28 and 29 indicate aluminum electrodes or wiring leads. In addition, numeral 30 indicates a surface oxide film of a poly-Si film.

The memory cell M-CEL has a double-layer poly-Si gate structure, in which a control gate 32 is stacked over a floating gate 31. Between the respectively adjacent gate structures, there are formed N^+ -type diffusion regions 33, 34 and 35, among which the region 33 is connected to a data line 36 of a aluminum.

As described above, the high voltage system of the peripheral circuitry is entirely constructed of the N-channel MISFETs disposed on the substrate 1 itself, and it does not include elements disposed within the well as in the CMOS already described. Therefore, even when the high voltage V_{PP} is applied to the diffused region, the situation where the well potential fluctuates does not occur at all, and the latch-up phenomenon based

on such fluctuation can be prevented. More specifically, if the high voltage system were fabricated of CMOS, P^+-type source and drain regions would be disposed within an N-type well. When such P^+-type regions exist, the well potential fluctuates on the application of the high voltage and the fluctuation acts as a triggering source, as already described, so that a P-N-P-N thyristor formed between the P^+-type regions and, for example, N^+-type diffused regions on the memory cell side is rendered conductive. In contrast, the construction according to the present embodiment does not include such a thyristor structure. Moreover, although carriers generated on the application of the high voltage in the high voltage system of the present embodiment are released through the substrate 1 itself, the distance through which they move is only as long as the thickness of the substrate 1, and hence, the resulting voltage drop is small. The potential fluctuation of the substrate 1 is accordingly small, so that latch-up is not likely to occur between the high voltage system and the FET Q_4 of the low voltage system.

In this connection, in the CMOS of the low voltage system, the N-type well 3 is fixed at the low voltage (5 V), and potential fluctuations are not likely to occur therein. Therefore, no triggering source exists in the well region, and latch-up can be satisfactorily prevented. In consequence, the peripheral circuit potions of the present embodiment become stable also in

the writing - reading switching operation as a whole.

Further, since the high voltage system has the structure formed with no well as described above, the size of the element area can be reduced to that extent, and enhancement in the density of integration can be attained.

The pull-up resistor R shown in Figure 2 may be formed of, for example, a high resistance poly-Si film which is disposed over the substrate 1 on an insulating film. Alternatively, a P-channel MISFET structure wherein such poly-Si film is selectively doped with an impurity so as to form P^+-type source and drain regions and wherein the poly-Si part between the two regions is used as a channel, may well be formed on the substrate 1. In this MISFET structure, the channel portion may be made low in resistance by rendering the MISFET conductive in the writing mode and high in resistance by bringing it into the nonconductive state in the reading mode, but the channel portion may well be doped with an impurity and formed into a load resistor of the depletion mode. Anyway, the P-channel MISFET is isolated from the substrate 1. Therefore, it is not feared at all that the latch-up described before will take place through the substrate 1 on application of the high voltage V_{pp}.

Since, in the present embodiment, the memory cells are entirely formed of N-channel MISFETs, switching FETs as in the case of forming memory cells of P-channel MISFETs are quite unnecessary. Also in this sense, the

density of integration can be enhanced.

The peripheral circuits according to the present embodiment exhibit sufficient breakdown voltages especially in the writing mode. If a still higher breakdown voltage is desired, the offset gate structure shown in Figure 4 can be adopted.

In, for example, the MISFET Q_1, the gate is constructed of the first layer of poly-Si film 9 and a second layer of poly-Si film 37 partly overlapping the film 9, and a low concentration N^--type region 38 is disposed on the drain side of the poly-Si film 9 in a manner to adjoin the high concentration N^+-type region 5. Both the second layer of poly-Si film 37 and the drain region 5 are set at the high voltage V_{pp}, or a separate voltage is applied to the poly-Si film 37. Thus, the high electric field of the drain is moderated by a depletion layer which extends from the P-N junction between the low concentration region 38 and the substrate 1, so that the quantity of carriers from the side of the source region 4 or the quantity of holes to be released from the P-N junction portion into the substrate 1 decreases. Therefore, the negative resistance attributed to the concentration of the carriers on the drain side lessens, and the source - drain breakdown voltage BV_{DS} rises.

Now, a method of manufacturing the EPROM shown in Figure 3 will be described with reference to Figures 5A - 5I.

First, as shown in Figure 5A, an N-type well 3 and

a field SiO_2 film 2 are respectively formed in and on one major surface of a substrate 1 by ion implantation and drive diffusion and by the selective oxidation technique employing an Si_3N_4 film 39 as a mask. For brevity of illustration, P^+-type channel stoppers are omitted (also in Figure 3).

Subsequently as shown in Figure 5B, the Si_3N_4 film 39 and the underlying SiO_2 film 40 are successively removed by etching, whereupon gate oxide films 16 are formed in respective element areas by a gate oxidation technique such as thermal oxidation. Further, a mask 41 of photoresist or the like is provided in a predetermined pattern, and an ion beam 42 of arsenic is implanted in a low dose, to form a shallow ion-implanted region 6 for a MISFET of the depletion mode. The mask 41 may well be such that an SiO_2 film on the surface of the substrate 1 is provided with a step. In this case, the ions may be implanted through only the thin SiO_2 parts.

Subsequently, as shown in Figure 5C, a first layer of poly-Si film grown on the whole surface by the chemical vapor deposition technique (hereinbelow, termed "CVD") is phosphorated (doped with phosphorus impurity), and it is thereafter patterned by the photoetching technique so as to leave a poly-Si film 43 covering the whole surface of the memory cell portion and the respective gate electrodes 9, 10 and 11 of the MISFETs of a high voltage application circuit, being a peripheral circuit.

Next, as shown in Figure 5D, thin SiO_2 films 17 are grown on the surfaces of the respective poly-Si films 9 - 11 and 43 by the thermal oxidation technique, a second layer of poly-Si film 44 is thereafter formed on the whole surface by the CVD process, and the poly-Si film 44 is further doped with phosphorus (phosphorated).

Next, as shown in Figure 5E, photoresist 45 is exposed to light and developed into a mask of predetermined pattern, which overlies the high voltage system-circuit portions of the peripheral circuit portions. Etching is performed for both the poly-Si films 44 and 43 of the memory cell portion, the poly-Si film 44 on the low voltage system-circuit portions of the peripheral circuit portions and the SiO_2 films 17 and 16. Thus, poly-Si films 32 and 31 of the double-layer gate structure are left in the memory cell portion, and poly-Si films 25 and 26 in the shape of gate electrodes are left in the peripheral low voltage circuit portions.

Subsequently, as shown in Figure 5F, the memory cell portion and the peripheral low voltage system-circuit portions are now covered with different photoresist 46, which is used as a mask for etching the poly-Si film 44 and SiO_2 films 17 and 16 of the high voltage system-circuit portions in succession.

At the next step, as shown in Figure 5G, a thin SiO_2 film is grown by the thermal oxidation technique

so as to extend from the surfaces of the respective poly-Si films to the exposed surface of the substrate 1, whereupon the well 3 of the peripheral low voltage system-circuit portion is covered with photoresist 47, a part of which is removed. In this state, an ion beam 48 of arsenic is implanted in a high dose so that the ions may be selectively implanted into predetermined regions by employing as a mask the poly-Si films 9 - 11, 25, 26, 31 and 32, the field SiO_2 film 2 and the photoresist 47. In this way, N^+-type source or drain regions 4, 5, 7, 8, 19, 20, 33, 34 and 35 of the respective FETs are formed on both the sides of the corresponding gate electrodes by the self-alignment method, and an N^+-type contact region 24 is formed in the well 3. As the aforementioned mask in the operation of implanting the ion beam of arsenic, an SiO_2 film formed by CVD may be used instead.

At the next step, as shown in Figure 5H, the substrate (except for parts of the well 3) is now covered with different photoresist 49, which is used as a mask for implanting an ion beam 50 of boron so that P^+-type source region 21 and drain region 23 may be respectively formed on either side of the poly-Si film 25 within the well 3. An SiO_2 film formed by CVD may be used instead as a mask for implanting the ion beam 50.

Subsequently, as shown in Figure 5I, a phosphosilicate glass film 18 deposited on the whole surface by CVD and the underlying SiO_2 films are successively

etched, to form respective contact holes. Next, aluminum is deposited on the whole surface by the vacuum evaporation technique and is thereafter patterned by the photoetching technique, to form the respective aluminum electrodes or wiring leads illustrated in Figure 3.

Figures 6A - 6C illustrate a method of forming the offset gate structure shown in Figure 4.

In forming this structure, the ion-implanted region 6 is formed in a somewhat larger area by the step of Figure 5B, whereby a low concentration N^--type ion-implanted region 6 which extends over the depletion mode FET Q_2 and the FET Q_1 is formed as shown in Figure 6A. In the same way as in Figures 5C - 5D, the gate electrodes 9 and 10 and the second layer of poly-Si film 44 are formed as shown in Figure 6A.

Subsequently, as shown in Figure 6B, by the step of Figure 5F and using the photoresist 46 as a mask, the second layer of poly-Si film is etched so as to be partly left while overlapping the poly-Si film 9. Then, the second layer of poly-Si film 37 in Figure 4 is formed.

Subsequently, as shown in Figure 6C, the SiO_2 films 17 and 30 are grown by thermal oxidation and the whole surface is irradiated with the ion beam of arsenic 48 in the same way as in Figure 5G. Thus, the arsenic ions are selectively implanted into regions where the poly-Si films 9, 10 and 37 do not exist, whereby the high concentration N^+-type regions 4, 5 and 7 are

respectively formed by self-alignment.

Since the subsequent steps are similar to those in Figures 5H - 5I, the explanation is omitted. It is important that the original ion implantation region 6 is, so to speak, divided by the N^+-type region 5 owing to the aforementioned ion implantation, so that one divided part is left as the channel portion of the depletion mode FET Q_2 and the other as the low concentration region 38 of the FET Q_1 which has the offset gate structure. Accordingly, the structure of Figure 4 has the low concentration region 38 thereof formed in common with the ion implanted region 6 of the FET Q_2 by the identical ion implantation step, and it is fabricated into the final configuration without altering the steps of Figures 5A - 5I, as described with reference to Figures 6A - 6C. Therefore, the manufacturing process is simple, and the job efficiency is high.

In contrast, in the case where the peripheral circuit of the high voltage system is fabricated of CMOS as already stated, attaining a high breakdown voltage as in Figure 4 requires that the low concentration (namely, P^--type) regions be formed on one side of the gate electrode on the P-channel side as well as on the N-channel side. In this case, the regions can be formed on the N-channel side in the way described with reference to Figures 6A - 6C, but the P^--type regions on the P-channel side need the step of implanting another species of ions (for example, boron ions), so that the

number of steps increases and the job efficiency is lowered accordingly.

While the foregoing embodiments have been described by way of example, numerous other embodiments of the invention can easily be envisaged. For example, the gate electrodes of the peripheral circuit portions in low voltage application circuits may be formed of the first layer of poly-Si film, and the respective gate electrodes can also be formed of a different material. In addition, when the ratio between the channel width and the channel length of the depletion mode FET Q_2 of the writing circuit is made small, current in the reading operation can be reduced. Further, this depletion mode FET Q_2 may be replaced with a high resistance element. In this case, the current in the reading operation diminishes. The present invention is applicable, not only to EPROMs, but also to other ROMs, e.g. those whose writing operations are electrically performed, for example, an EEPROM (electrically erasable and programmable ROM).

CLAIMS:

1. A semiconductor memory device comprising:

a P-type semiconductor body;

a memory cell portion which includes a plurality of non-volatile memory cells formed in a part of said semiconductor body; and

a peripheral circuit portion which is formed in parts of said semiconductor body that are not provided with said non-volatile memory cells and which includes a first circuit portion made of circuit elements arranged to be energized by a first voltage and a second circuit portion made of circuit elements arranged to be energized by a second voltage lower than said first voltage;

said circuit elements of said first circuit portion being first insulated gate type FETs which have N-type channels and, are formed directly in the semiconductor body while said circuit elements of said second circuit portion are a plurality of pairs of second insulated gate type FETs, each of which pairs comprises a P-channel FET and an N-channel FET.

2. A semiconductor memory device according to claim 1, wherein said first voltage is the writing voltage, and said second voltage is the reading voltage.

3. A semiconductor memory device according to claim 1 or claim 2, wherein said first circuit portion includes a writing circuit.

4. A semiconductor memory device according to any one of the

preceding claims, wherein said second circuit portion includes an input/output buffer.

5. A semiconductor memory device according to any one of the preceding claims, wherein said second circuit portion includes a decoder.

6. A semiconductor memory device according to any one of claims 1 to 5, wherein a field insulating film is formed on parts of said semiconductor body between adjacent non-volatile memory cells and between adjacent circuit elements of said peripheral circuit portion, and wherein those of said second insulated gate type FETs which have P-type channels are formed in an N-type well region which is formed in said semiconductor body.

7. A semiconductor memory device according to claim 6, wherein said field insulating film is an SiO_2 film.

8. A semiconductor memory device according to claim 1 or claim 6 or claim 7, wherein each of said non-volatile memory cells has stacked gates, and each of said first and second insulated gate type FETs has a single gate.

9. A semiconductor memory device according to claim 8, wherein said stacked gates of each non-volatile memory cell consist of two layers of polycrystalline silicon.

10. A semiconductor memory device according to any one of claims 6 to 9, wherein said first insulated gate

type FET has a gate electrode which is made of a first polycrystalline silicon film and a second polycrystalline silicon film partly overlapping said first polycrystalline silicon film.

11. A semiconductor memory device according to claim 10, wherein said first insulated gate type FET includes a low impurity concentration N-type semiconductor region which is formed under said second polycrystalline silicon film, and a drain region which adjoins said low impurity concentration semiconductor region and which has a higher impurity concentration than this semiconductor region.

12. A semiconductor memory device substantially as described herein with reference to and as illustrated in Figs. 1 to 3 and 5, or Figs. 4 and 6 of the accompanying drawings.

13. A method of manufacturing a semiconductor memory device according to any one of the preceding claims, comprising:

the step of forming a field insulating film on selected areas of one major surface of a P-type semiconductor body, said field insulating film isolating said one major surface of said semiconductor body into at least first, second and third areas;

the step of forming an N-type well region in a part of said first area so as to leave a body region in another part of said first area;



the step of forming a first polycrystalline silicon layer on said three areas, and selectively removing said first polycrystalline layer to leave a plurality of gate electrodes on said second area and a first polycrystalline silicon film on said third area;

the step of forming an insulating film on the surfaces of said plurality of gate electrodes and said first polycrystalline silicon film respectively formed on said second area and said third area;

the step of forming a second polycrystalline silicon layer on the first, second and third areas;

the step of selectively removing said second polycrystalline silicon layer and said first polycrystalline silicon film to form a plurality of gate electrodes on said well and body regions of said first area and to form gate electrodes of memory cells on said third area,

the step of introducing an N-type impurity into said body region of said first area, and said second and third areas by using as a mask said plurality of gate electrodes formed on said body region of said first area and on said second and third areas, thereby to form a plurality of N-type semiconductor regions;

the step of introducing a P-type impurity into said well region of said first area by using as a mask said gate electrode formed on said well region;

the step of forming an insulating film on said first, second and third areas and selectively removing this insulating film, thereby to form contact holes; and

the step of forming wiring leads which connect with said plurality of semiconductor regions through said contact holes.

14. A method of manufacturing a semiconductor memory device according to claim 13, wherein said first and second polycrystalline silicon films are formed by chemical vapor deposition.

15. A method of manufacturing a semiconductor memory device according to claim 13 or claim 14, wherein said step of introducing the N-type impurity into said first, second and third areas by using said plurality of gate electrodes as the mask is carried out by ion implantation.

16. A method of manufacturing a semiconductor memory device according to any one of claims 1 to 12, substantially as described herein with reference to the accompanying drawings.