CLAIMS

What is claimed is:

1. A semiconductor apparatus, comprising:

a first semiconductor layer;

a second die;

a thermally conductive layer, wherein the thermally conductive layer is stacked with the first semiconductor layer and the second die, is located between the first semiconductor layer and the second die, and is configured to conduct heat from the first semiconductor layer and/or heat from the second die at the thermally conductive layer, and a coefficient of thermal conductivity of the thermally conductive layer in a horizontal direction is greater than or equal to a coefficient of thermal conductivity in a vertical direction, and a surface of the thermally conductive layer facing the first semiconductor layer and a surface facing the thermally conductive layer comprise an insulating material; and

a first conductive pillar, wherein the first conductive pillar penetrates through the thermally conductive layer, so that the first semiconductor layer and the second die are electrically interconnected by using the first conductive pillar, the first conductive pillar is electrically insulated from the thermally conductive layer, an extension direction of the first conductive pillar is the vertical direction, and the coefficient of thermal conductivity of the thermally conductive layer in the horizontal direction is greater than a coefficient of thermal conductivity of the first semiconductor layer.

2. The semiconductor apparatus according to claim 1, wherein there are a plurality of vias at the thermally conductive layer, and one or more first conductive pillars penetrate through one of the vias.

3. The semiconductor apparatus according to claim 1 or 2, wherein there is a bonding-based connection between the thermally conductive layer and the first semiconductor layer.

4. The semiconductor apparatus according to any one of claims 1 to 3, wherein the insulating material covers the surface of the thermally conductive layer, and the first conductive pillar further penetrates through the insulating material.

5. The semiconductor apparatus according to any one of claims 1 to 4, further comprising:

an insulation layer, wherein the insulation layer is disposed to at least partially surround the

first conductive pillar and extend along the first conductive pillar and is configured to isolate the first conductive pillar from the thermally conductive layer to implement electrical insulation.

6. The semiconductor apparatus according to claim 5, further comprising:

a filler material, wherein the filler material is disposed at the thermally conductive layer and is located between the thermally conductive layer and the insulation layer.

7. The semiconductor apparatus according to claim 6, wherein the filler material is compatible with a through silicon via (TSV) process, and a through silicon via refers to an electrical interconnection implemented by filling a via of a silicon wafer with a conductive material.

8. The semiconductor apparatus according to any one of claims 1 to 7, wherein the first semiconductor layer is a first die or a first interconnection layer.

9. The semiconductor apparatus according to any one of claims 1 to 8, wherein the first semiconductor layer is the first die, the first conductive pillar further penetrates through the first die.

10. The semiconductor apparatus according to claim 9, further comprising:

a third semiconductor layer, wherein the third semiconductor layer is disposed on a side that is of the first semiconductor layer and is far away from the thermally conductive layer, and is electrically coupled to the conductive pillar.

11. The semiconductor apparatus according to any one of claims 1 to 10, wherein the thermally conductive layer comprises a carbon-based material, a metal material, or a combination thereof.

12. The semiconductor apparatus according to claim 11, wherein the carbon-based material comprises a graphene film.

13. The semiconductor apparatus according to claim 1, wherein a thickness of the thermally conductive layer is at least 5 μm.

14. An electronic device comprising the semiconductor apparatus according to any one of claims 1 to 13.